UPDATE 2014

1. Introduction

2. New interface
    1. 10 Gb/s protocol (see Petr talk)
    2. FED optical protocol

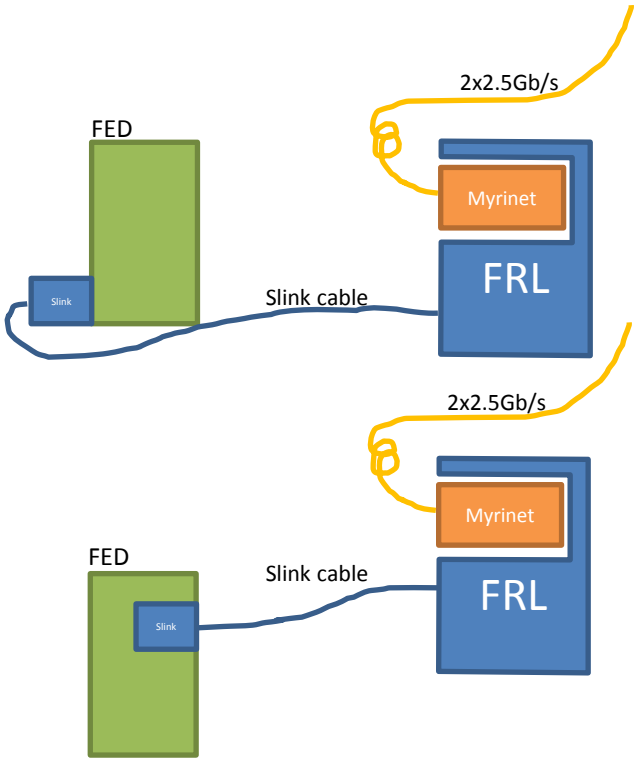
3. Fonctionality
    & Block diagram

4. Implementation(s)

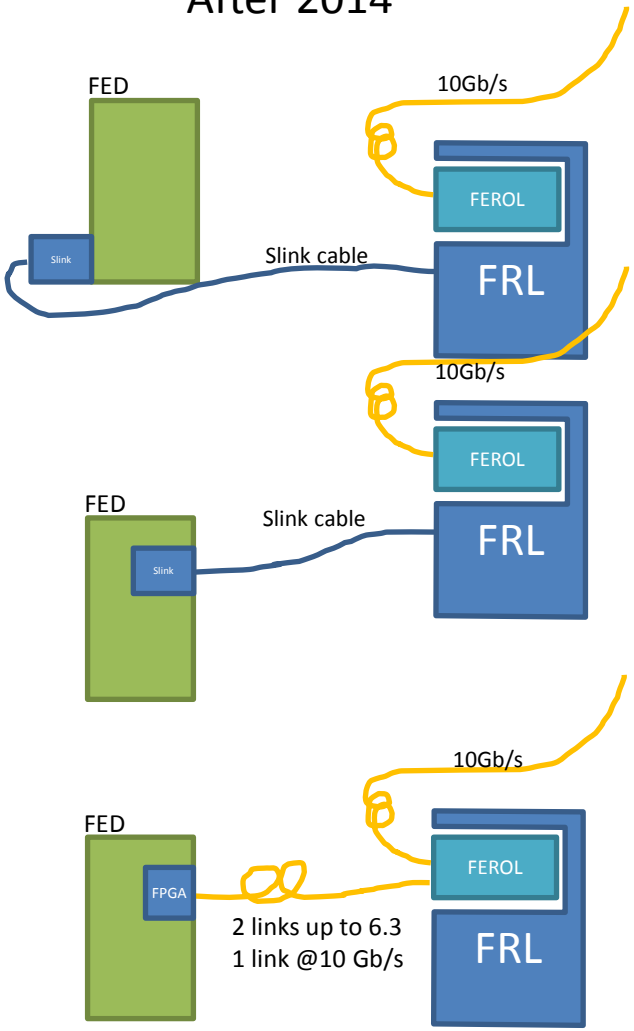
5. Conclusions

Introduction

Up to 2012



After 2014



IN

A new optical link up to 6.3Gb/s

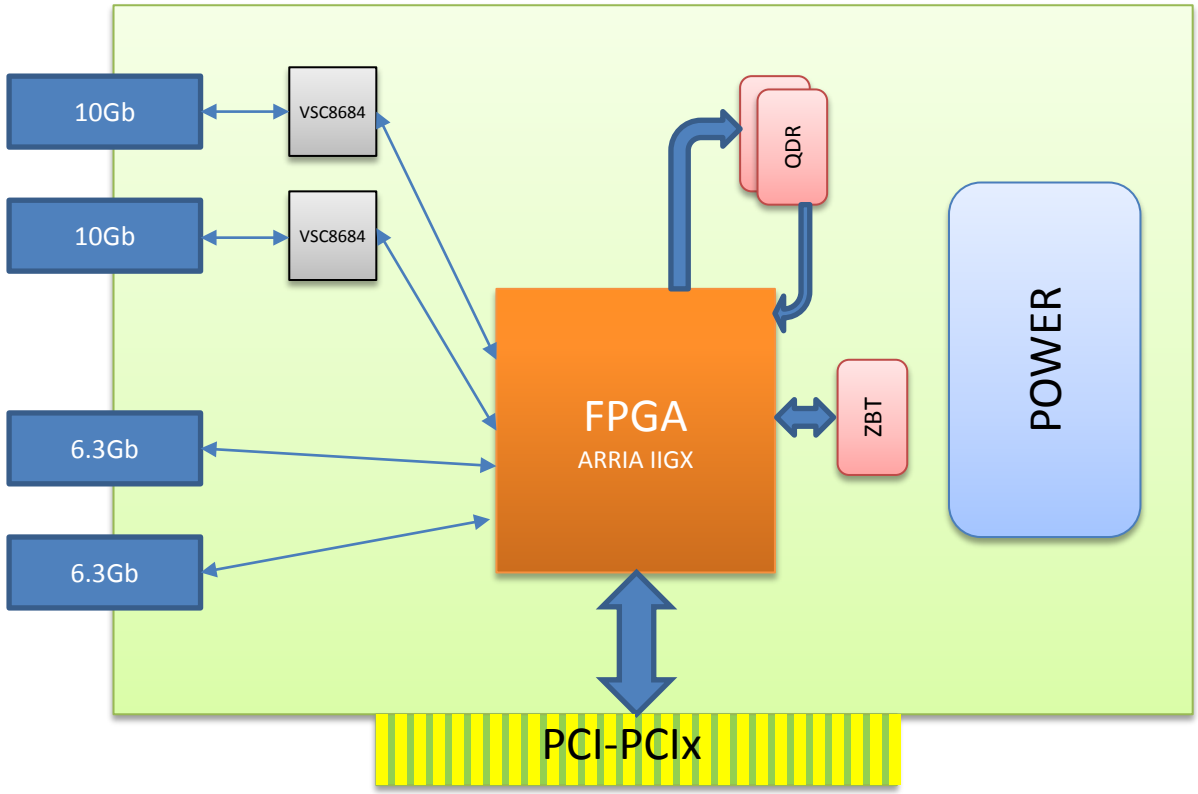
OUT

A new optical link @ 10 Gb/s (TCP)

New interface

Proto II:

PCI-x (to be sit on FRL)
QDR
ZBT
10Gb/s (2x IN-OUT)
6.3Gb/s (2x IN)



2 link 10Gb/s

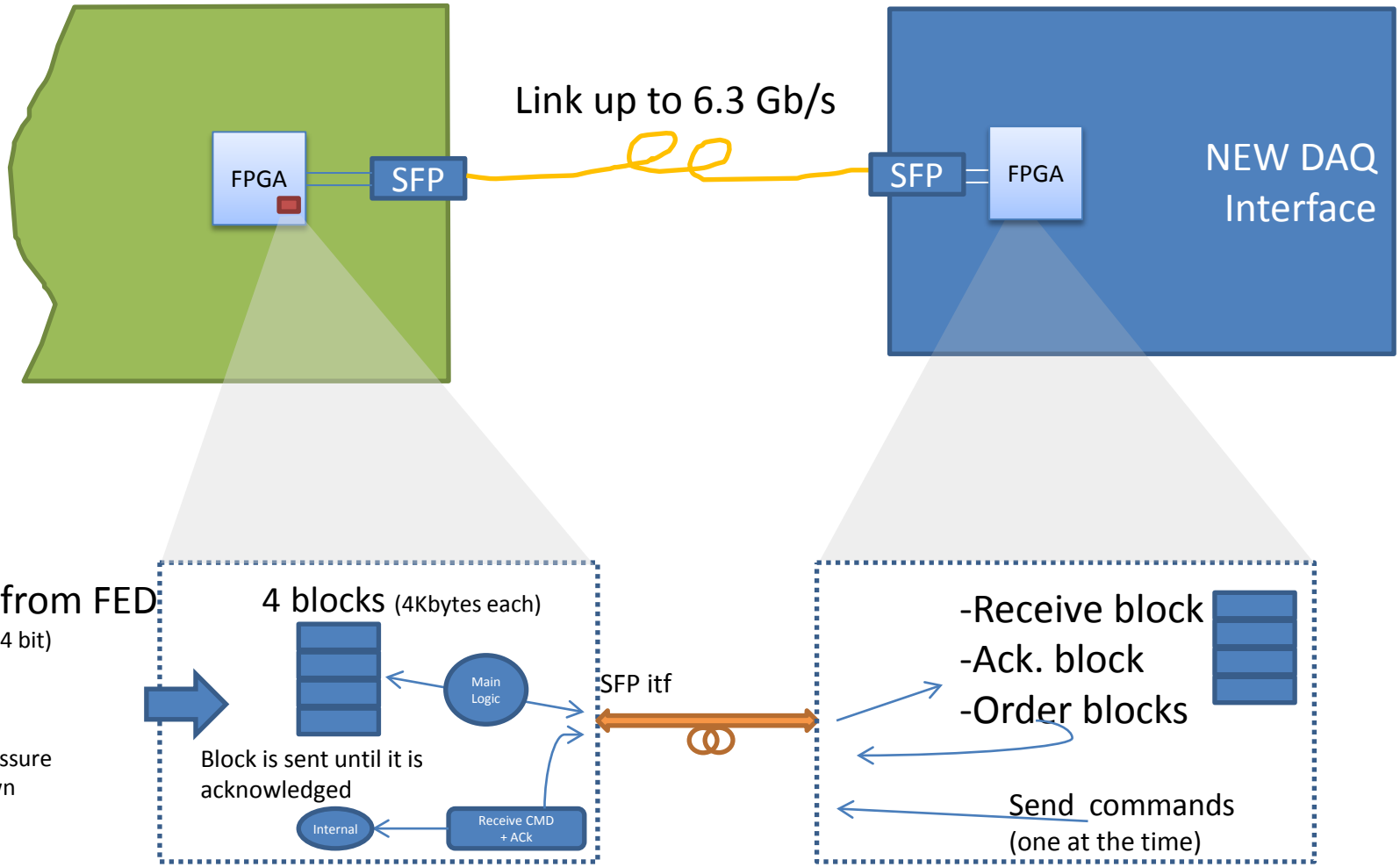
-1 x DAQ data link
-1 x multi purposes (redundant DAQ link or IN FED)

2 link up to 6.3 Gb/s

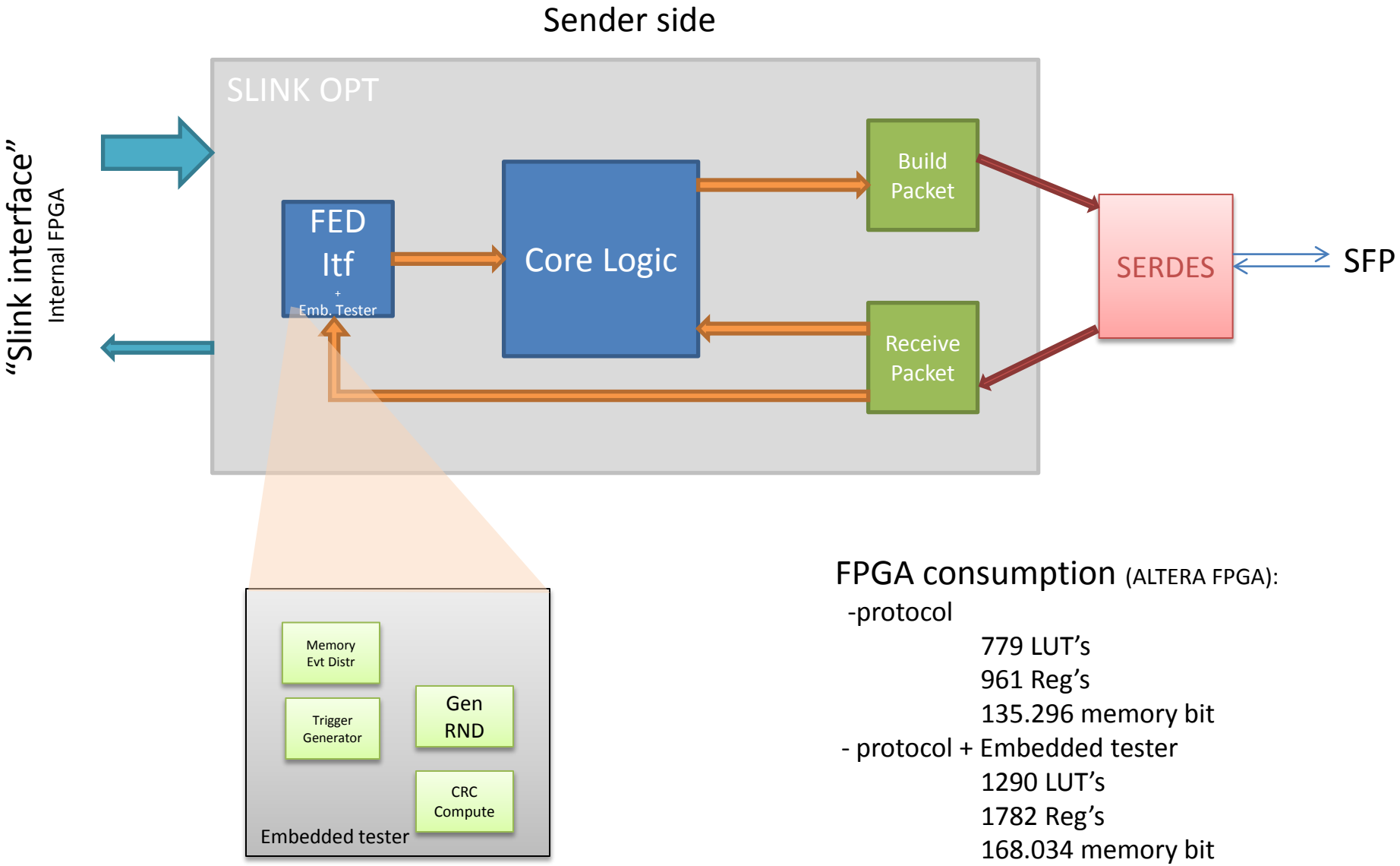
-2x IN FED

PCI-x 64b@100 MHz
For up to 2 SLINK connections

FED interface



Block diagram



FPGA consumption (ALTERA FPGA):

-protocol

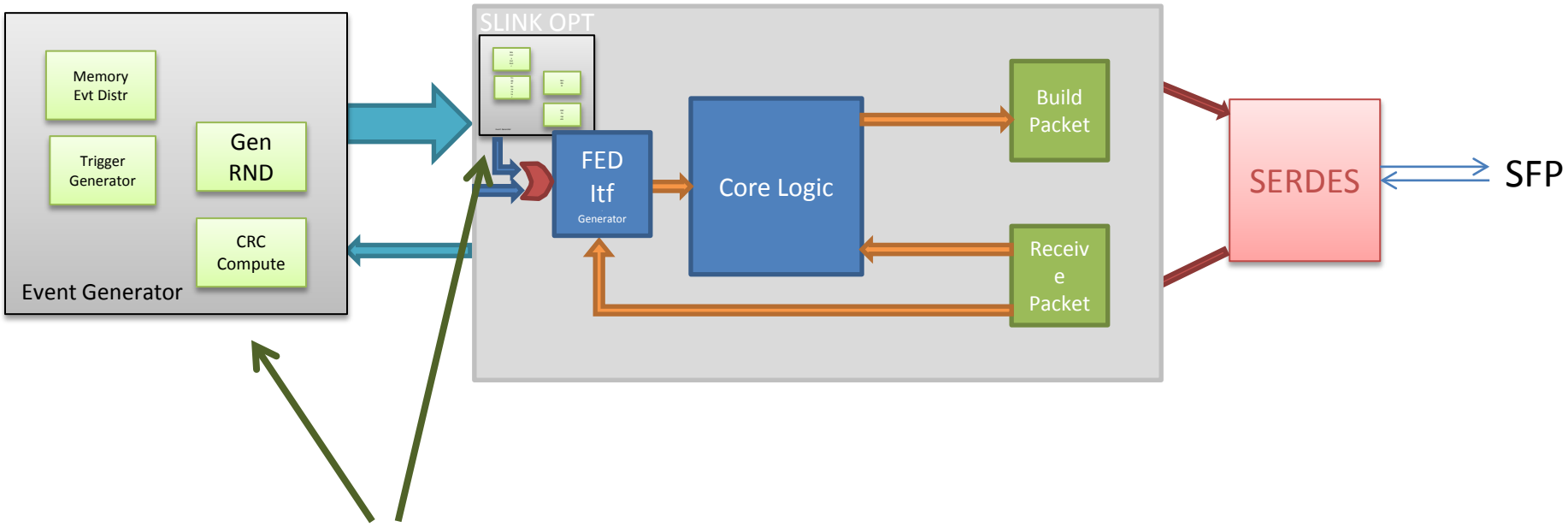
779 LUT's
961 Reg's
135.296 memory bit

- protocol + Embedded tester

1290 LUT's
1782 Reg's
168.034 memory bit

Sender implementation

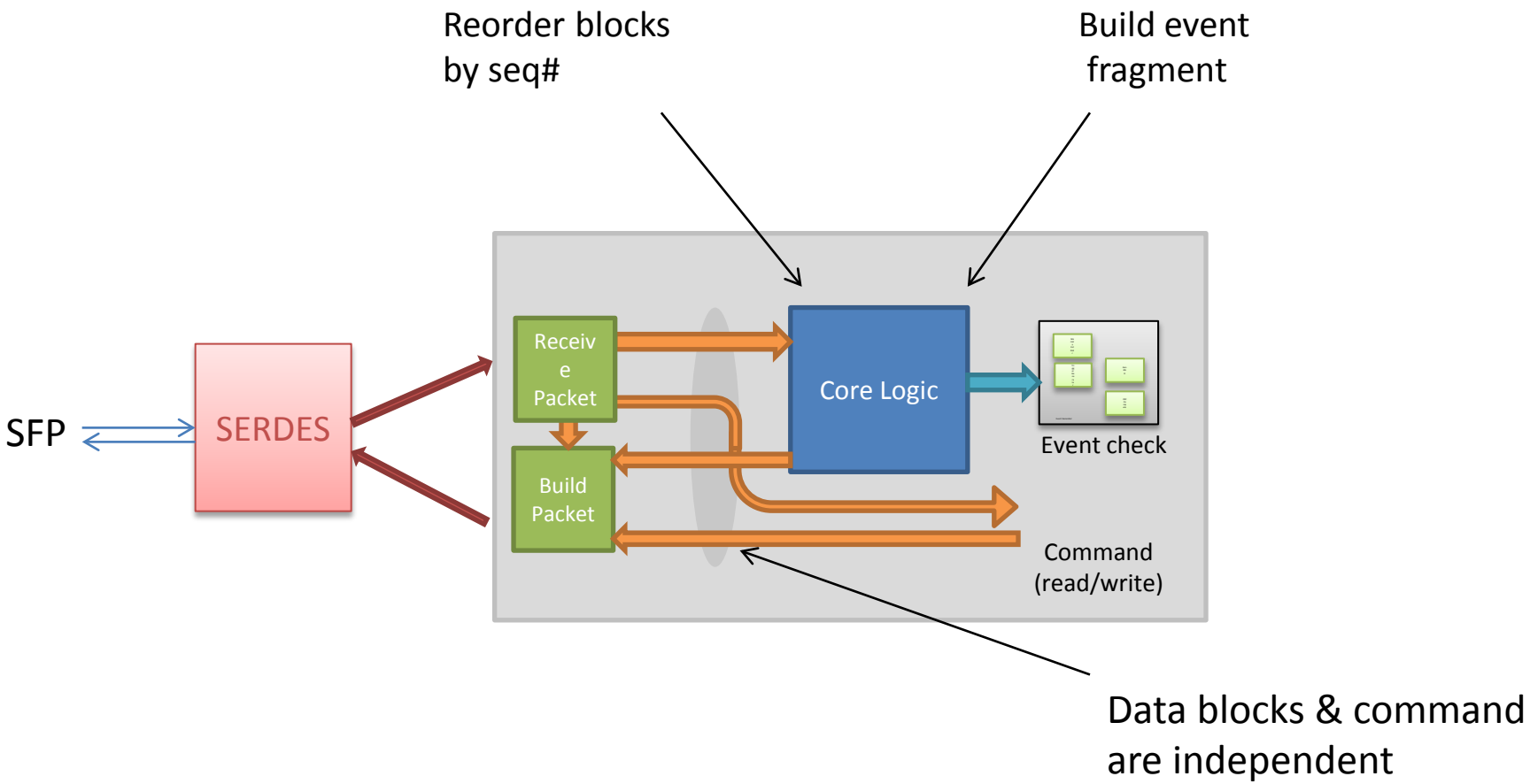
Sender side



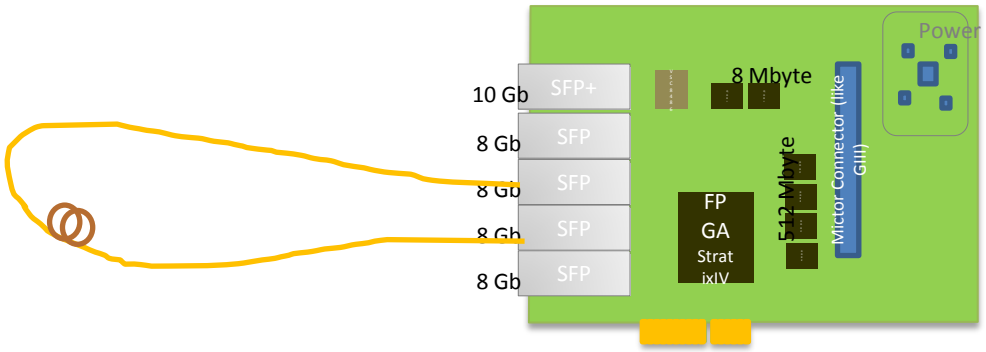
Two generators

- one to emulate the DATA FED
- one : embedded-tester

Receiver implementation

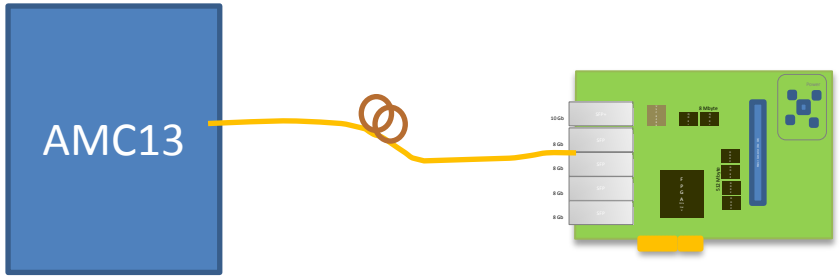


Implementation(s)



DONE

In progress



To be done

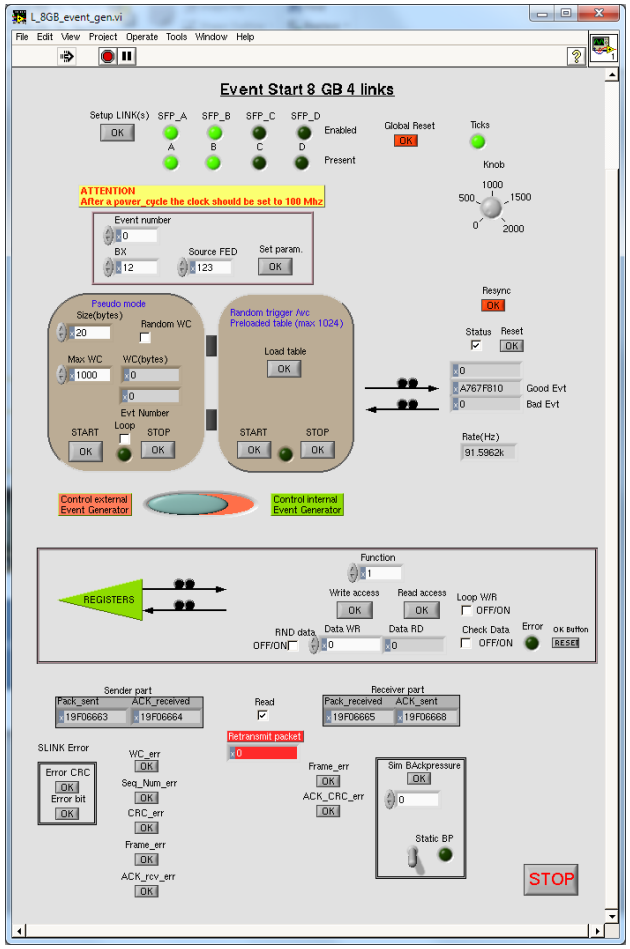
Tests

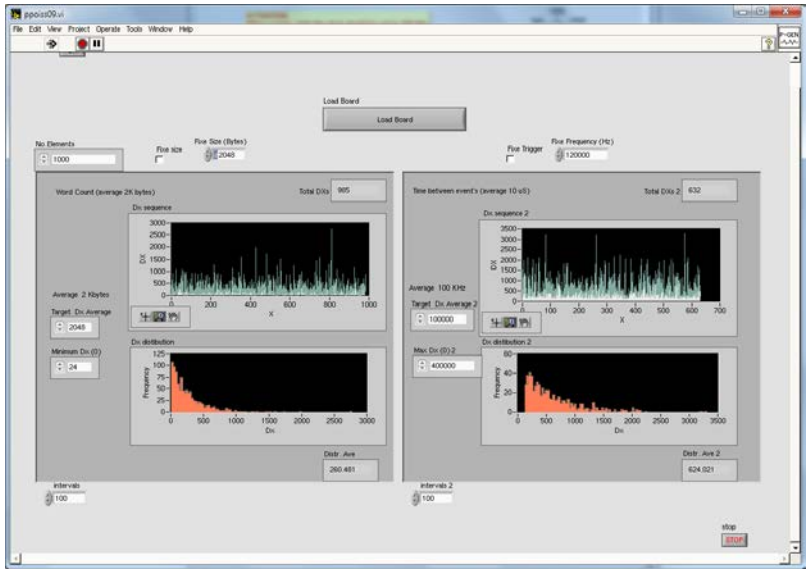
SFP control

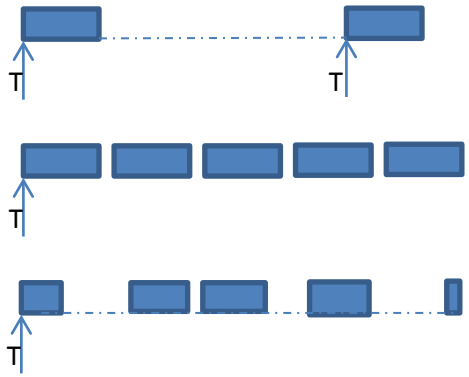
Event gen control
FED_emu &
Embedded tester

Command
From
DAQ side

Error generator







Single event
(Fixed size or random size)

Loop events
(Fixed size or random size)

Events with
Preloaded size and trigger distribution

Error generator:

- Acknoledge (send –receive)
- Error on fragment- CRC- size
-Backpressure emulator

Conclusions

-New prototype (FEROL = Front-End Readout Optical Link)

-Schematic	: done
-PCB routing	: in progress
-First PCB	: September
-Components sold	: October
- First debugging	: November
-Preserie	: launch in Mi-November to have 50 boards Jan 2013
-Production	: Feb 2013 to be ready to install for Nov. 2013

For TCP/IP protocol (tests and implemtation, see Petr talk)

-FED Optical protocol

Protocol and block is implemented and tested in ALTERA FPGA (Stratix IV)

Protocol and block is implemented in XILINX FPGA (XILINX kit ML605)

Debugging starting now

Implementation and test in AMC13 as soon as the block is tested in XILINX kit

“Protocol details”

The protocol is based on 32-bit data path (using the 8/10 bit code)

During the idle state, the block send xBC7CDC1C (k= “1111”; all K bytes)

Each frame starts with x00FB (K= “01”)
And end with CRC and 0xFD00 (K = “10”)

All Bytes between have a means (data, Word-count,..)

Init frame:
Sequence number : 0x0000000 (32bit) bit 31 =0
LSC_ID: (16bit)
Length : 16bit = 0 for init

Command frame:
Sequence number : 0x0000000 (32bit) bit 31 =0
LDC_ID: (16bit)
Length : 16bit
Command (32 bit (bit31= 1 specify a write = 0 a read)
DATA (32-bit each)

Data frame:
Sequence number : 0x0000000 (32bit) bit 31 =0
LSC_ID: (16bit)
Length : 16bit
Command (64bit : specify the content of the frame)
DATA (64-bit each)

Ack frame:
Sequence number : 0x0000000 (32bit) bit 31 = 1
LDC_ID/LSC_ID: (16bit)
Reserved: 16bit
data(64 bit (data /status)