Universal PCI board

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1.Introduction

Many applications have to use PCI bus as communication way. Why PCI, because it is a standard that exits in many kind of machine (PC, Macintosh, SUN…..). To meet the maximum of applications, the PCI 64-bit 66MHz is the version adapted for a standard board. This kind of specification able the user to plug it inside a 33 MHz PCI bus or 66 MHz with 32-bit or 64-bit . The only care that has to be done is about the IO power. The 66Mhz PCI bus requires 3.3 volts. By the way, the FPGA used is only 3.3 volts compatible. **This board can't be used in a 5 volts PCI bus** (same if the PCI connector of the board able to do it).
This board is a transfert PCI bus to user bus that is on two kinds of connectors (PMC: Slink format and MICTOR).

Figure : Universal PCI board

The user can then develop a PMC that has one of those connectors.

2.Description

This board is built around one FPGA.
The board contains:

- -32Mbytes of SDRAM (64-bit word)
- -1Mbytes of FLASH ram (8-bit word)
- -user pins (PMC or MICTOR connectors)
- -PCI bus 32/64-bit @ 33/66MHz

Four different clocks can be use for user pins & SDRAM

a.-PCI clock 33 or 66MHz
b.-a quartz frequency (0 to 133 MHz)
c.-a quartz frequency (0 to 100 MHz)
d.-pin user connector (input)

The SDRAM can be synchronized with a, b, c or d.
User pins can be synchronized with a,c or d.
The two kind of connectors are:
-PMC Slink form factor. The specification of those connectors can be find :
http://cmsdoc.cern.ch/cms/TRIDAS/horizontal/docs/slink64.pdf
http://cmsdoc.cern.ch/cms/TRIDAS/horizontal/docs/s-link.pdf
-MICTOR connectors. Pins used with the previous connectors are connected also to the Mictor connectors + 64 user free pins.
For the both type of connectors , all defined and free user pins have a connection to the FPGA (bidirectional pins execpted for clocks).

3.Functions

The first funtionality implemented inside the FPGA is :

a. A SDRAM controller (synchronized with PCI) able to do burst of 8 words (32 or 64 bit word). The memory can be accessible indifferently in 32-bit or 64-bit access (PCI Base Address 1).
b. A FLASH memory controller that accept only single word access of 32-bit where only LSByte is used (PCI Base Address 2) .
c. A generator a random words (max 100MHz).

4. Generator Random Words (GRW)

To test the 64-bit 66MHz PCI in full speed, and to reach the maximum bandwidth of the PCI bus (512 MB/s), the FPGA include a generator of words (64-bit composed by 4 x 16-bit identical words).
The protocol is the following;
A controller has to write BA0 +4h the word-count (D15..D0) and the SEED of the Random Generator Engine (D31..D16). And to write at the BA0+8h the PC address memory where the GRW has to write the data generated.
The GRW will automatically start burst access corresponding to SEED WC and PC address memory. At the end an interrupt will be generated to indicate to the controller that the block transfer is finished.
The controller can read the interrupt register at the BA0+Ch (“1” interruption , “0” no interruption) and can clear it with a write to the BA0+Ch.
A control can be done to check the random data. The arithmetic form is:
X = seed At the begining
First time = SEED + 3 = OUT (t0)
OUT(t0) = (OUT(t-1) * 5) +3

5. Settings board

Some settings have to be done before using the board the first time

a. The user clock and the SDRAM clock have to be specified. In the schematic, on the page 4 we can see what is possible to do:

ST3 Close: the user clock (connector clock) is generated on board (Quartz or PCI)
Open: the user clock comes from I/O connector.
ST1 1-2 closed: the user clock is the PCI clock .
2-3 closed: the user clock is the Quartz Q1 (3.3 volts).
ST2 1-2 closed: the SDRAM clock is the Quartz Q2 (3.3 volts)
2-3 closed: the SDRAM clock is the PCI clock.
Those options able to design a synchronous logic or to have a logic much more faster inside the FPGA and for the I/O connectors.(Figure 2)

b. The second setting correspond to the JTAG chain. If there is no daughter board connected to connectors or the daughter board has no JTAG chain, the BYPASS_JTAG switch has to be set on ON (close). Otherwise if connectors close the JTAG chain , this switch has to be set on OFF (open).

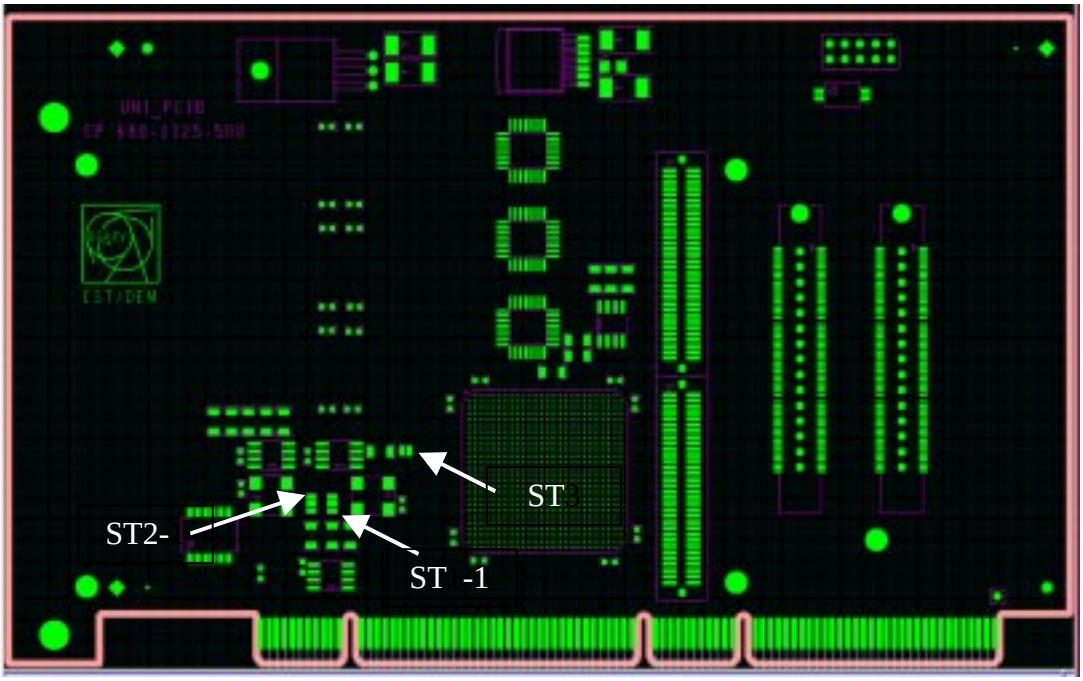

Figure 2