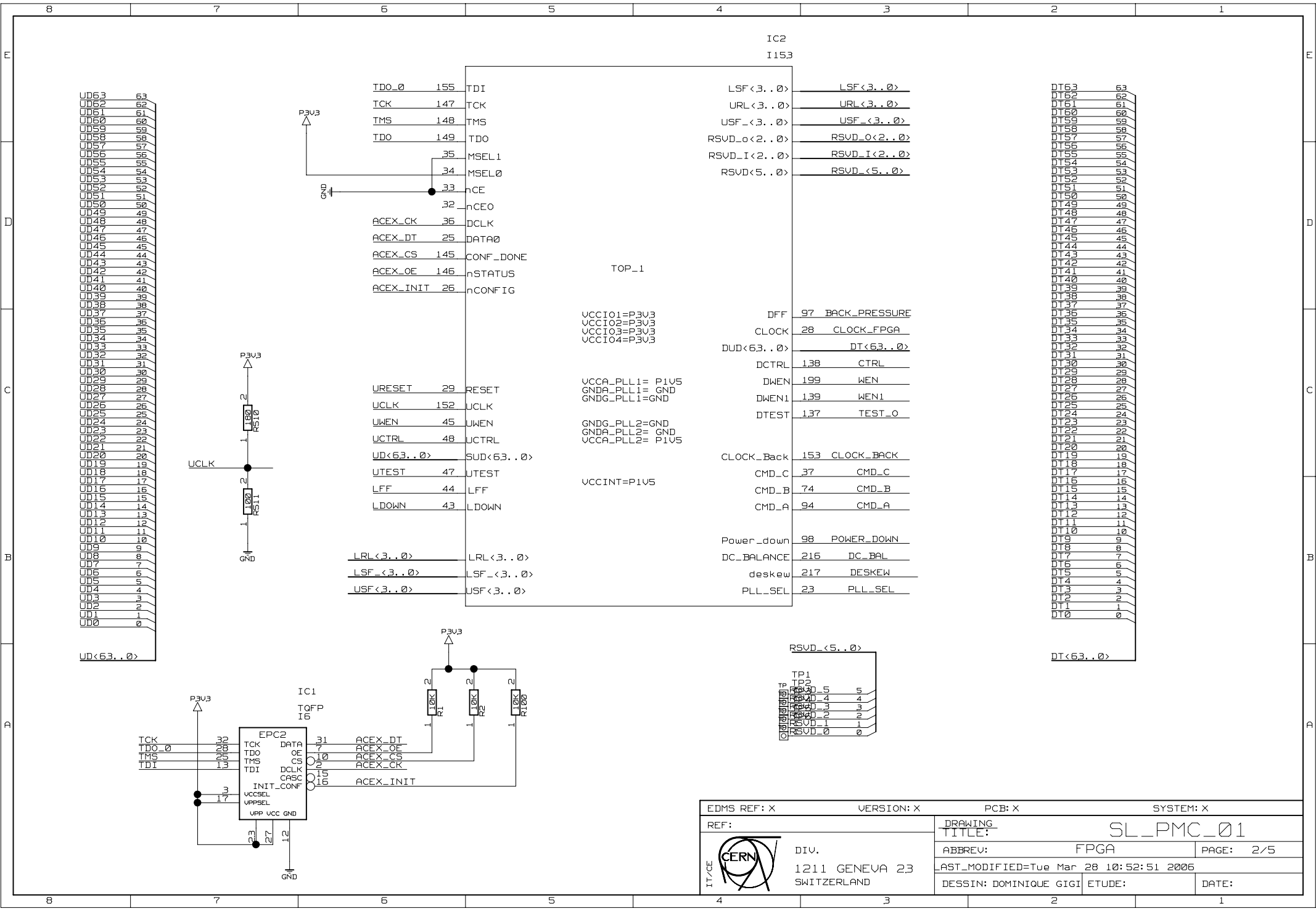


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		LAST_MODIFIED= Tue Mar 28 17:43:29 2006		DESSIN: DOMINIQUE GIGI ETUDE:			
IT/CE		DATE:					



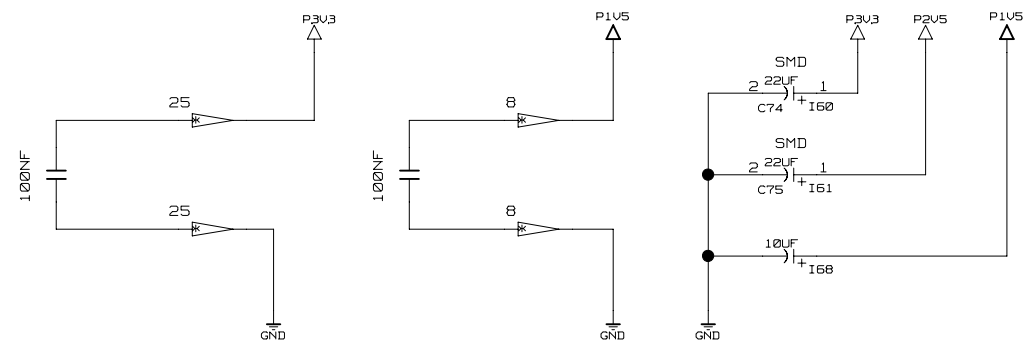
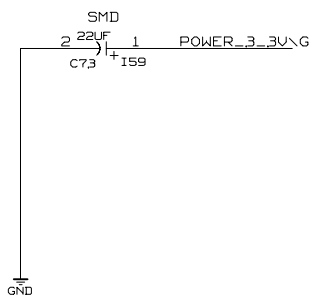
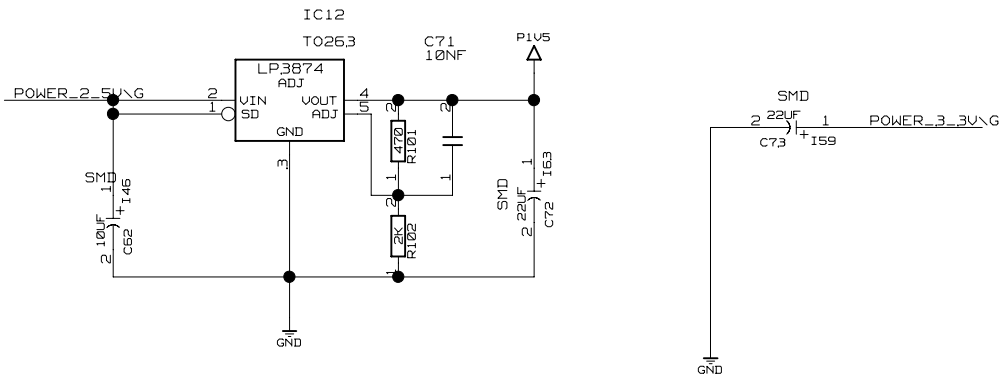
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ABBREU: FPGA		AST_MODIFIED=		Tue Mar 28 10:52:51 2006		DATE:	
DESSIN: DOMINIQUE GIGI		ETUDE:					



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DIV.  
1211 GENEVA 23  
SWITZERLAND





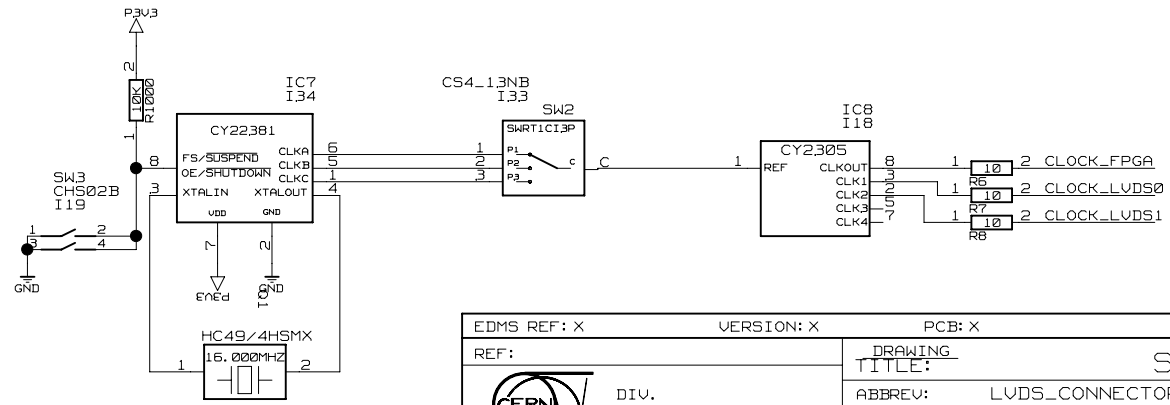
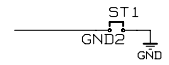



GND=GND2  
 (43, 44, 42)  
 (GND: 41)

J3

TXOUTN00	1	1	21	21	TXOUTP00
TXOUTN01	2	2	22	22	TXOUTP01
TXOUTN02	3	3	23	23	TXOUTP02
TXCLKN0	4	4	24	24	TXCLKP0
TXOUTN03	5	5	25	25	TXOUTP03
TXOUTN04	6	6	26	26	TXOUTP04
TXOUTN05	7	7	27	27	TXOUTP05
	8	8	28	28	
RXCLKP	9	9	29	29	RXCLKN
RXINP1	10	10	30	30	RXINN1
RXINP0	11	11	31	31	RXINN0
RXINP2	12	12	32	32	RXINN2
	13	13	33	33	
TXOUTN10	14	14	34	34	TXOUTP10
TXOUTN11	15	15	35	35	TXOUTP11
TXOUTN12	16	16	36	36	TXOUTP12
TXCLKN1	17	17	37	37	TXCLKP1
TXOUTN13	18	18	38	38	TXOUTP13
TXOUTN14	19	19	39	39	TXOUTP14
TXOUTN15	20	20	40	40	TXOUTP15

MDR40RARS



EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE:		SL_PMC_01		PAGE: 5/5	
 DIV. 1211 GENEVA 23 SWITZERLAND		LAST_MODIFIED= Tue Mar 28 17:50:54 2006 DESSIN: DOMINIQUE GIGETUDE:		DATE:			