


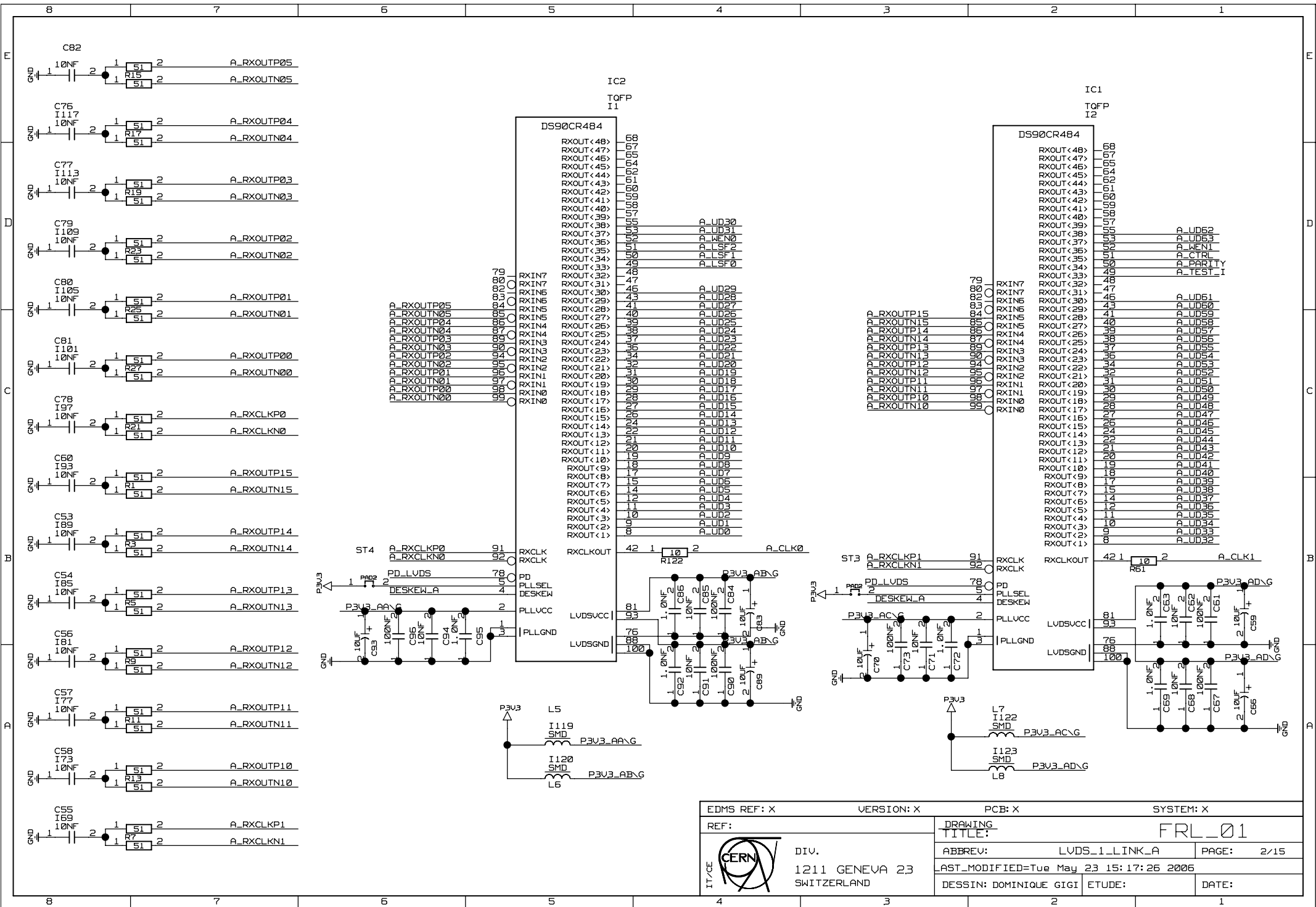
PCI-J1 WITH SHIELD REV 3.0


AD_PC31	E6	AD31	TRST	C1
AD_PC30	A7	AD30	TCK	A2
AD_PC29	B7	AD29	TMS	D2
AD_PC28	C7	AD28	TDO	F2
AD_PC27	E7	AD27	TDI	F2
AD_PC26	A8	AD26		
AD_PC25	D8	AD25		
AD_PC24	E8	AD24		
AD_PC23	C9	AD23		
AD_PC22	E9	AD22		
AD_PC21	A10	AD21		
AD_PC20	D10	AD20		
AD_PC19	E10	AD19		
AD_PC18	A11	AD18		
AD_PC17	B11	AD17		
AD_PC16	C11	AD16		
AD_PC15	B19	AD15		
AD_PC14	C19	AD14		
AD_PC13	E19	AD13		
AD_PC12	A20	AD12		
AD_PC11	D20	AD11		
AD_PC10	E20	AD10		
AD_PC9	B21	AD9		
AD_PC8	C21	AD8		
AD_PC7	A22	AD7		
AD_PC6	D22	AD6		
AD_PC5	E22	AD5		
AD_PC4	B23	AD4		
AD_PC3	C23	AD3		
AD_PC2	E23	AD2		
AD_PC1	A24	AD1		
AD_PC0	D24	AD0		

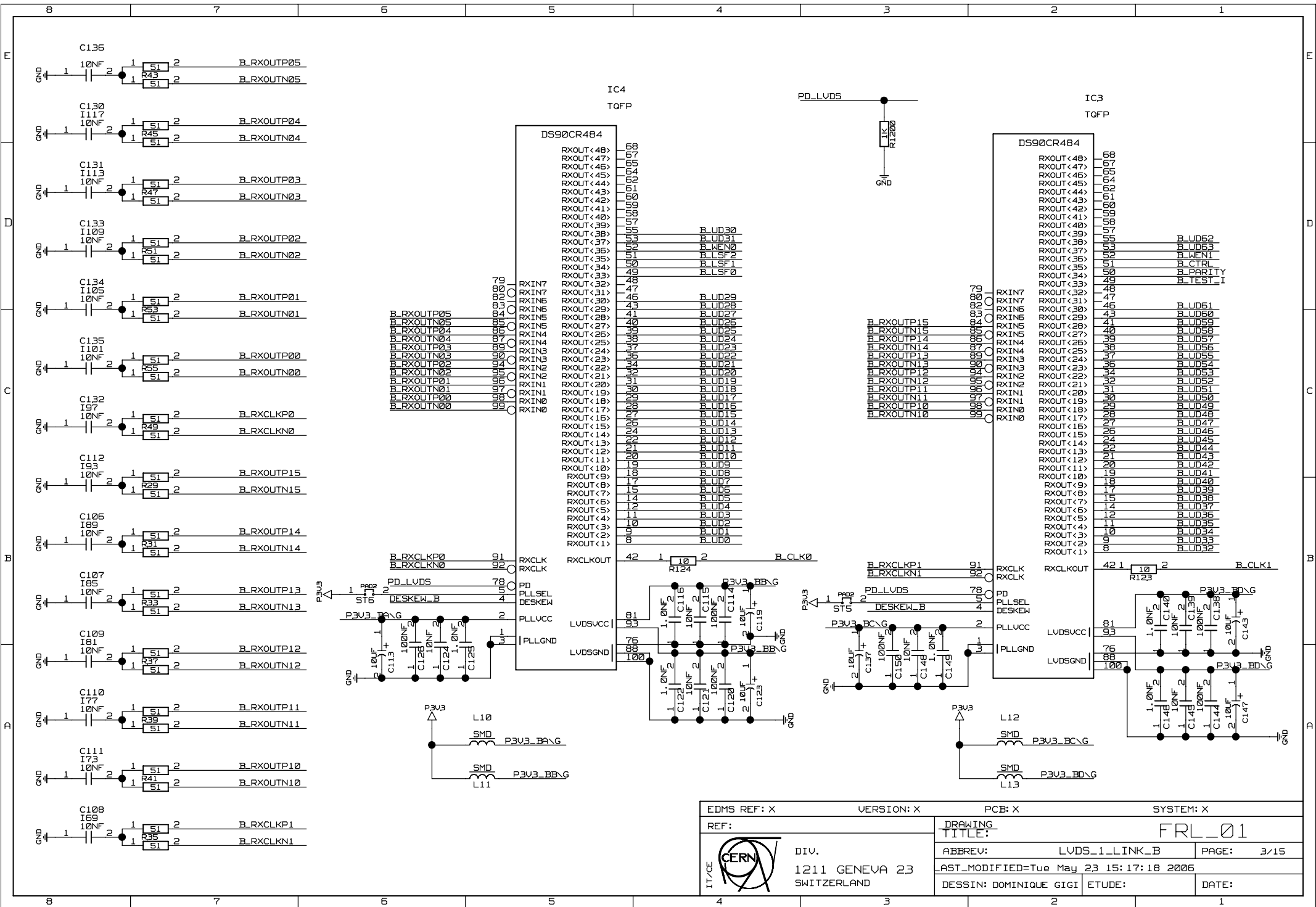
J7
I1.33

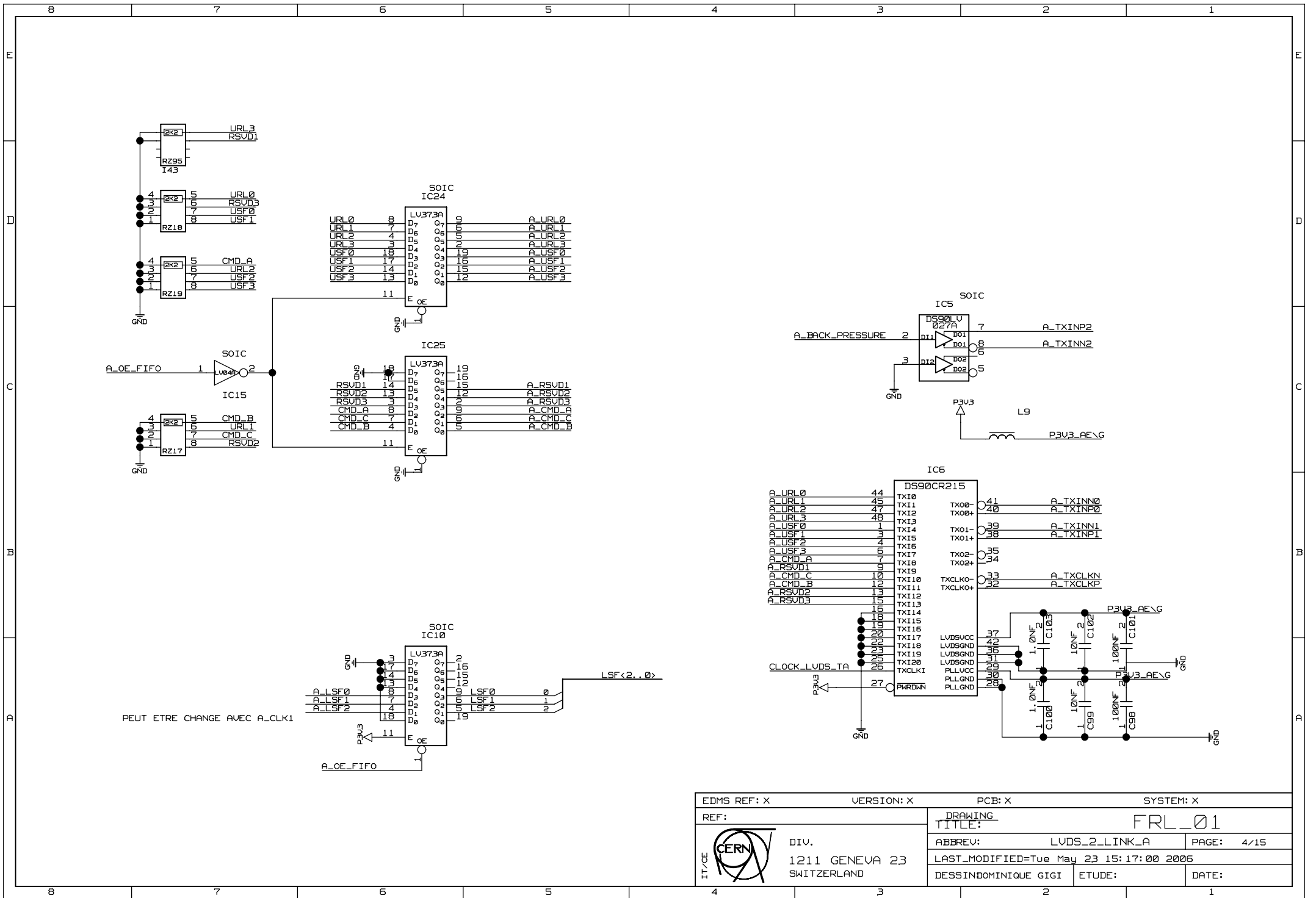
J6
I1.34

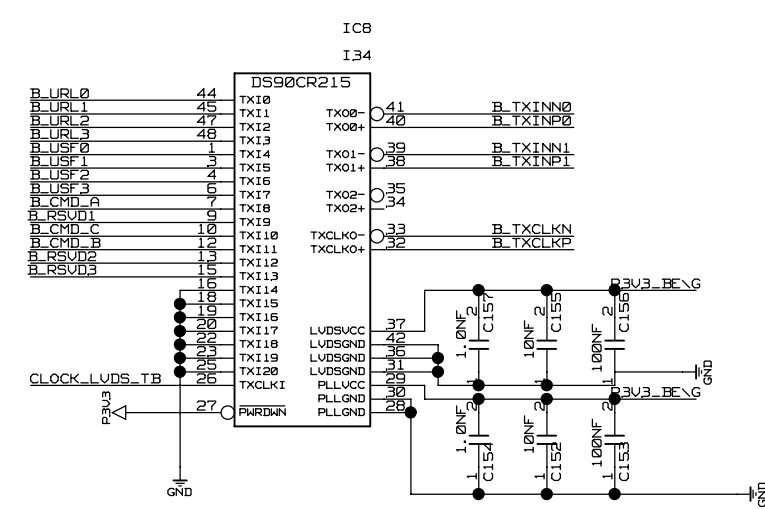
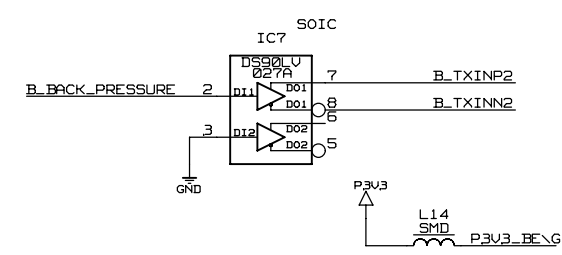
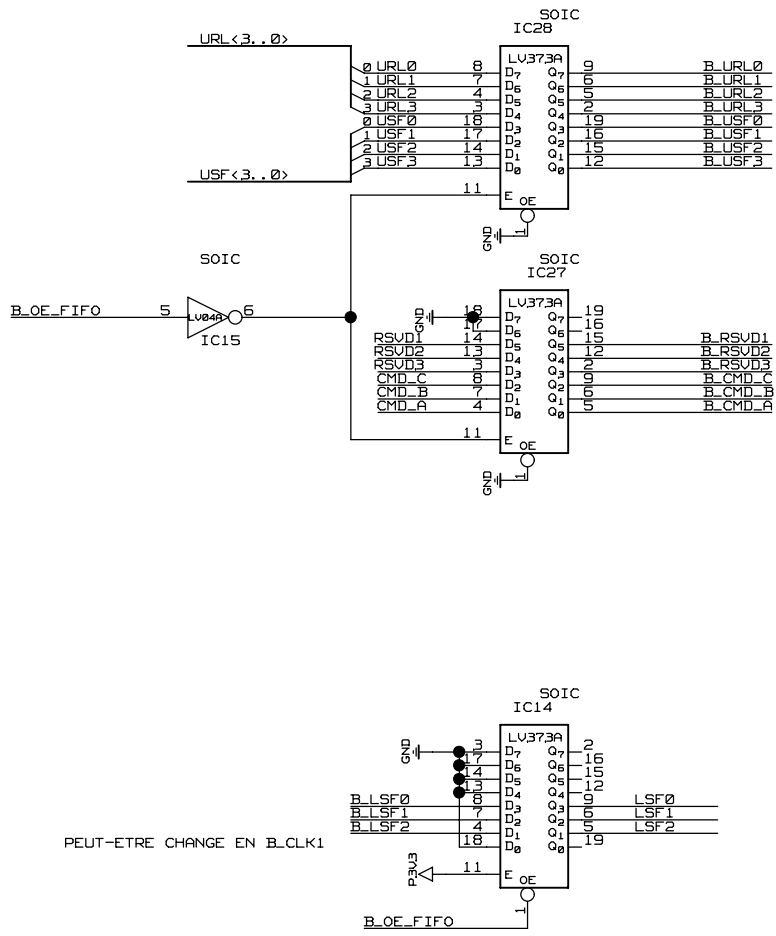
EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE: FRL_01		PAGE: 1/15
 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: COMPACTPCI_CONNECTOR	DATE:	
	AST_MODIFIED= Tue May 23 14:47:21 2006		
DESSIN: DOMINIQUE GIGI		ETUDE:	




EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE:		FRL_01		PAGE: 2/15	
 DIV. 1211 GENEVA 23 SWITZERLAND		ABBREV: LVDV_1_LINK_A AST_MODIFIED= Tue May 23 15:17:26 2006		DESSIN: DOMINIQUE GIGI		ETUDE: DATE:	

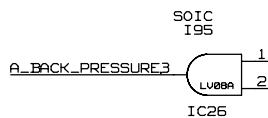
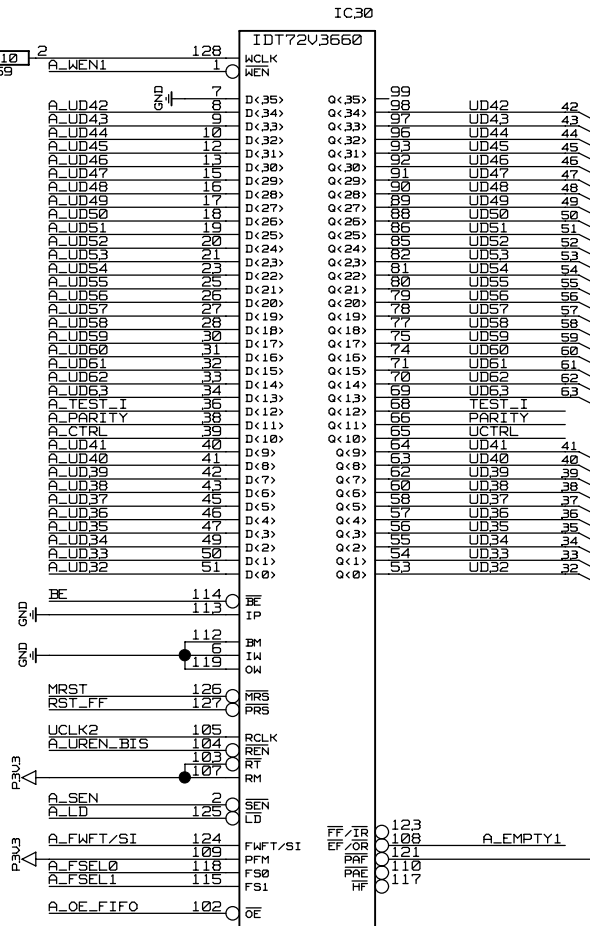
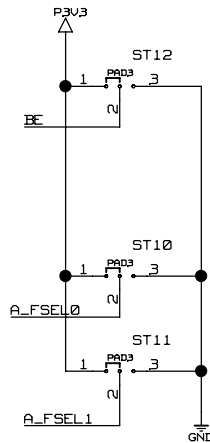
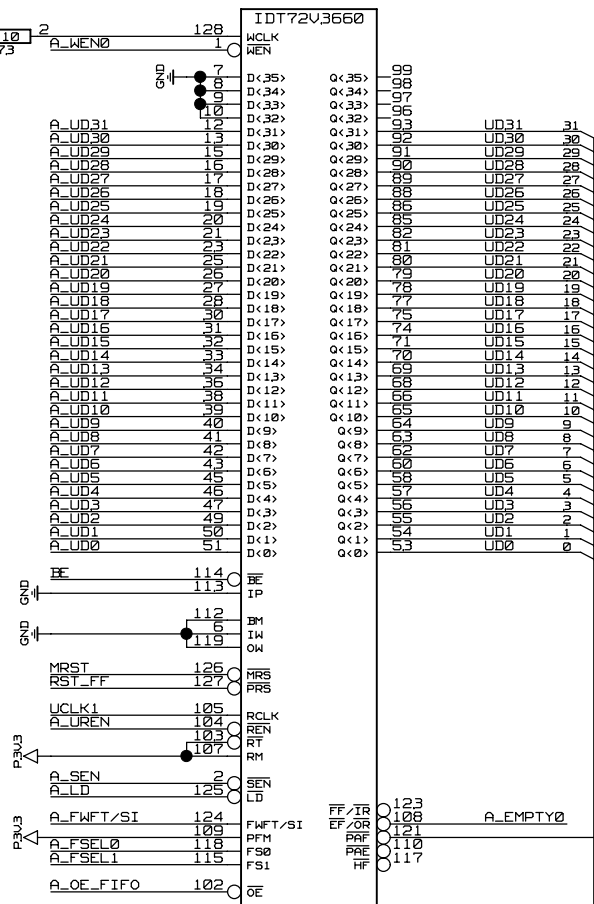
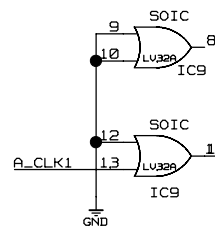
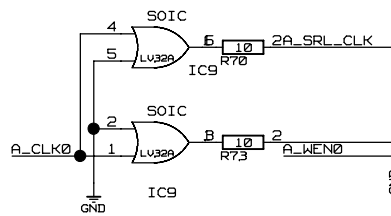





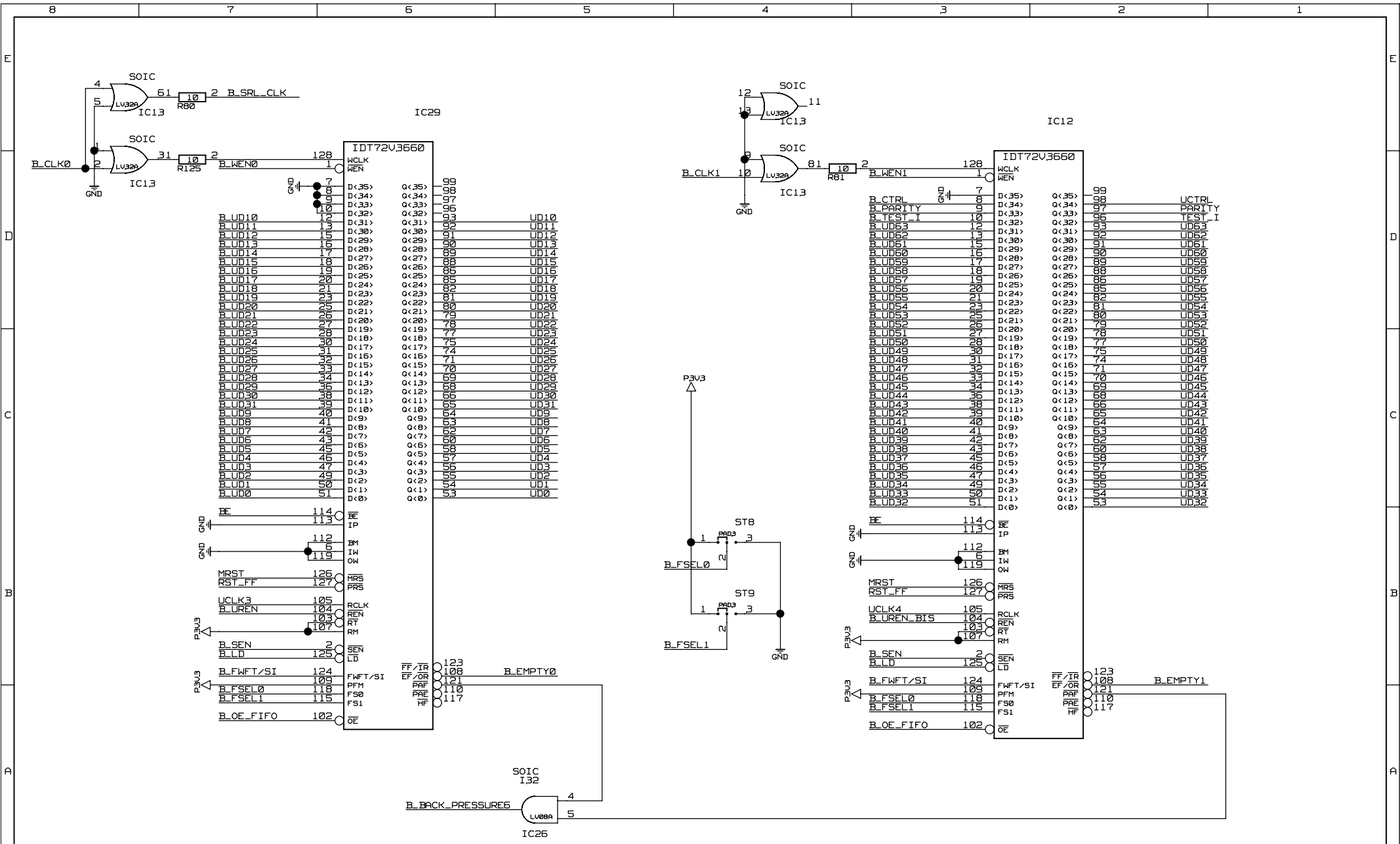



PEUT-ETRE CHANGE EN B_CLK1

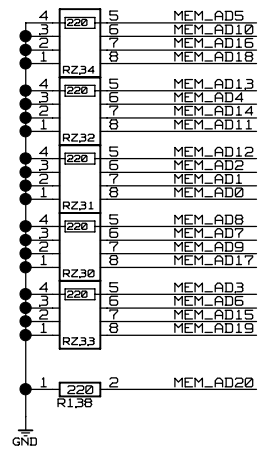
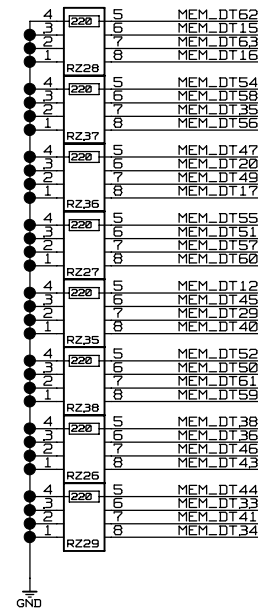
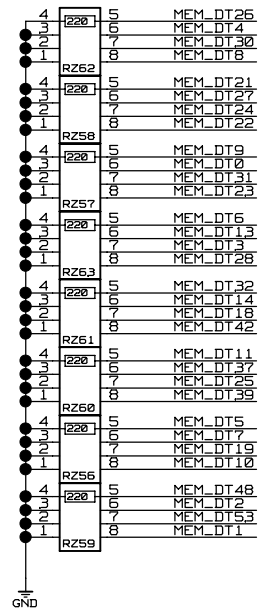
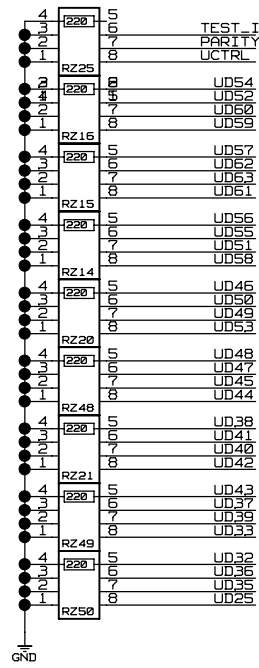
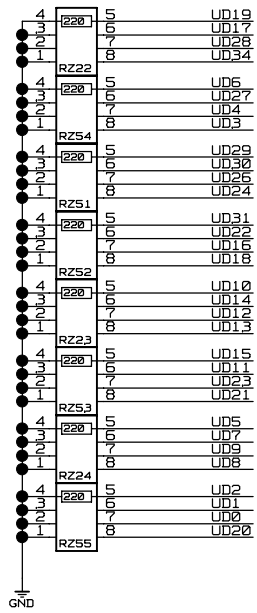
EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE: FRL_01				PAGE: 5/15	
 DIV. 1211 GENEVA 23 SWITZERLAND		ABBREU: LVDS_2_LINK_B		LAST_MODIFIED= Tue May 23 15:00:30 2006		DESSINDOMINIQUE GIGI	
		DATE:		ETUDE:		DATE:	




EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE: FRL_01		PAGE: 6/15
 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: BUFFER_LINK_A	DATE:	
	LAST_MODIFIED: Mon Sep 20 08:44:36 2004	DESSIN: DOMINIQUE GIGI	ETUDE:



EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE:		FRL_01		PAGE: 7/15	
 DIV. 1211 GENEVA 23 SWITZERLAND		ABBREV: BUFFER_LINK_B LAST_MODIFIED=Mon Sep 20 08:44:36 2004		DESSIN: DOMINIQUE GIGI ETUDE:		DATE:	



EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE:		FRL_01		PAGE: 8/15	
 DIV. 1211 GENEVA 23 SWITZERLAND		ABBREV: PULL_DOWN_NETWORK		AST_MODIFIED=Mon Sep 20 08:44:36 2004		DATE:	
		DESSIN: DOMINIQUE GIGI		ETUDE:			

(43, 44, 41)

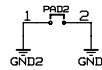
<GND: 42>

GND=GND2

J2

I11

		MDR40RARS			
B_RXOUTN00	1	1 21	21	B_RXOUTP00	
B_RXOUTN01	2	2 22	22	B_RXOUTP01	
B_RXOUTN02	3	3 23	23	B_RXOUTP02	
B_RXCLKN0	4	4 24	24	B_RXCLKP0	
B_RXOUTN03	5	5 25	25	B_RXOUTP03	
B_RXOUTN04	6	6 26	26	B_RXOUTP04	
B_RXOUTN05	7	7 27	27	B_RXOUTP05	
	GND	8 28	28		GND
B_TXINN0	9	9 29	29	B_TXINP0	
B_TXINN1	10	10 30	30	B_TXINP1	
B_TXCLKN	11	11 31	31	B_TXCLKP	
B_TXINN2	12	12 32	32	B_TXINP2	
	GND	13 33	33		GND
B_RXOUTN10	14	14 34	34	B_RXOUTP10	
B_RXOUTN11	15	15 35	35	B_RXOUTP11	
B_RXOUTN12	16	16 36	36	B_RXOUTP12	
B_RXCLKN1	17	17 37	37	B_RXCLKP1	
B_RXOUTN13	18	18 38	38	B_RXOUTP13	
B_RXOUTN14	19	19 39	39	B_RXOUTP14	
B_RXOUTN15	20	20 40	40	B_RXOUTP15	
	GND	41 41	41		GND



(43, 44, 41)

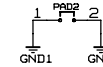
<GND: 42>

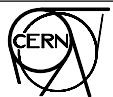
GND=GND1

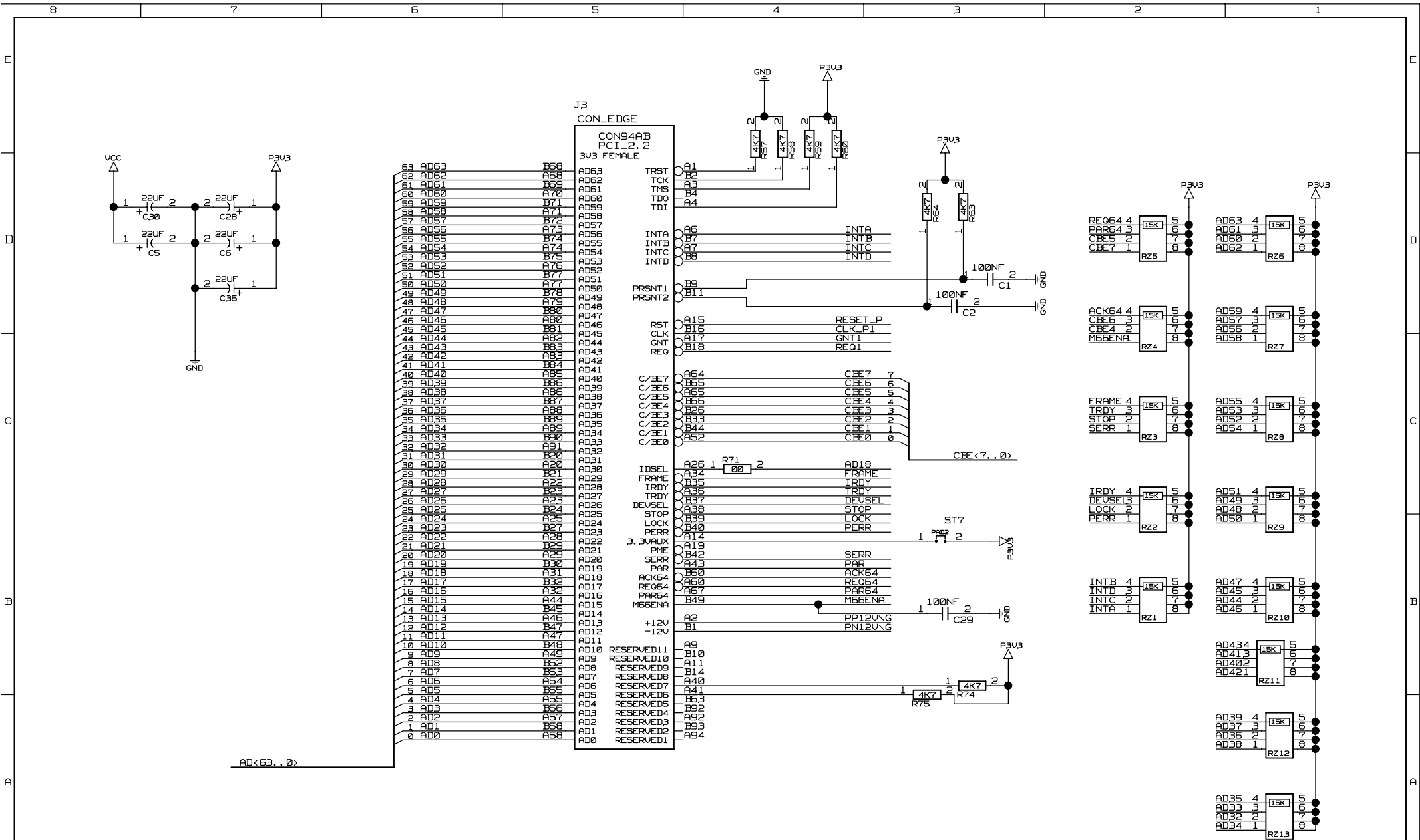
J1


I1

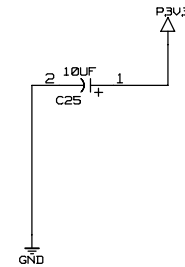
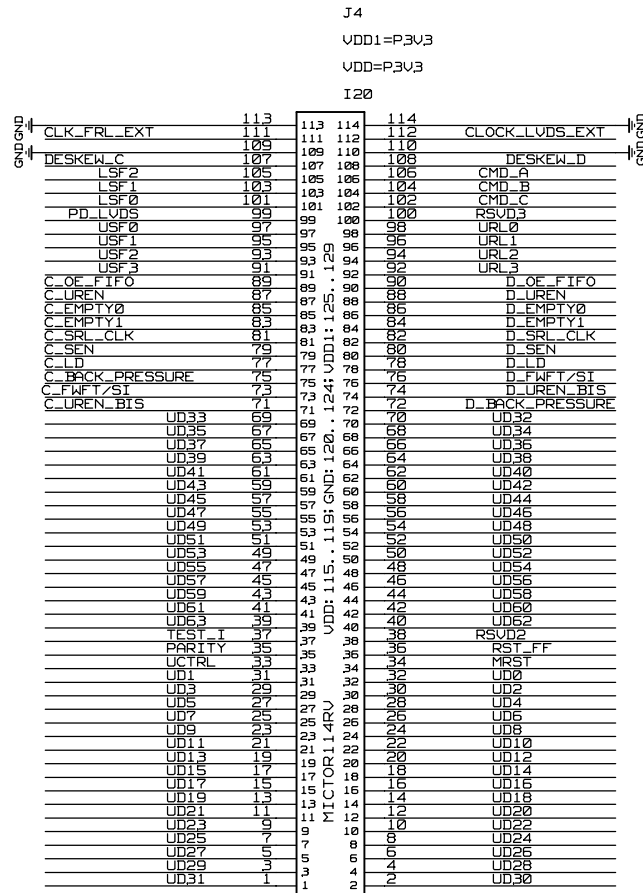
		MDR40RARS			
A_RXOUTN00	1	1 21	21	A_RXOUTP00	
A_RXOUTN01	2	2 22	22	A_RXOUTP01	
A_RXOUTN02	3	3 23	23	A_RXOUTP02	
A_RXCLKN0	4	4 24	24	A_RXCLKP0	
A_RXOUTN03	5	5 25	25	A_RXOUTP03	
A_RXOUTN04	6	6 26	26	A_RXOUTP04	
A_RXOUTN05	7	7 27	27	A_RXOUTP05	
	GND	8 28	28		GND
A_TXINN0	9	9 29	29	A_TXINP0	
A_TXINN1	10	10 30	30	A_TXINP1	
A_TXCLKN	11	11 31	31	A_TXCLKP	
A_TXINN2	12	12 32	32	A_TXINP2	
	GND	13 33	33		GND
A_RXOUTN10	14	14 34	34	A_RXOUTP10	
A_RXOUTN11	15	15 35	35	A_RXOUTP11	
A_RXOUTN12	16	16 36	36	A_RXOUTP12	
A_RXCLKN1	17	17 37	37	A_RXCLKP1	
A_RXOUTN13	18	18 38	38	A_RXOUTP13	
A_RXOUTN14	19	19 39	39	A_RXOUTP14	
A_RXOUTN15	20	20 40	40	A_RXOUTP15	
	GND	41 41	41		GND




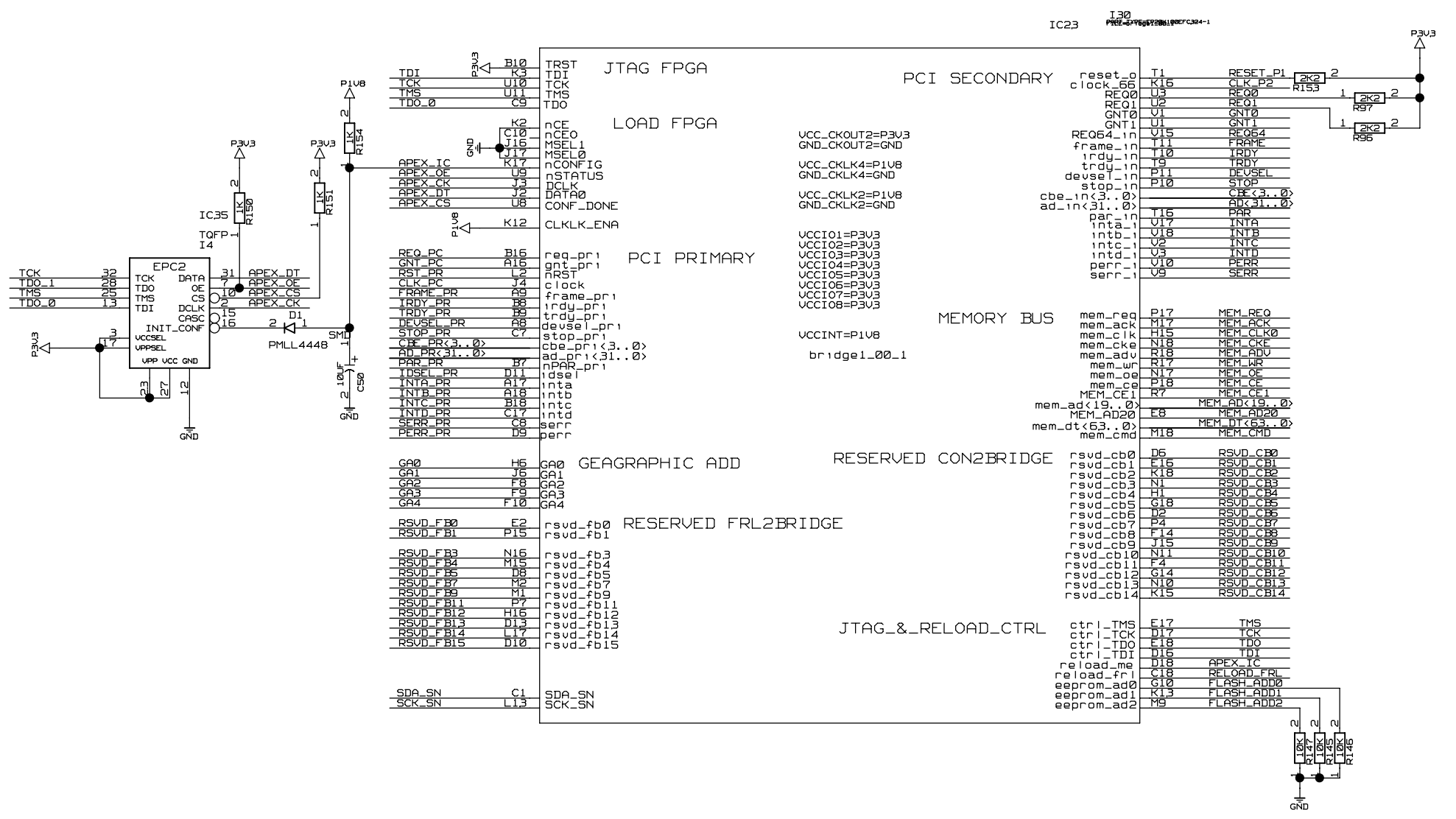
EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE: FRL_01				PAGE: 9/15	
IT/CE 	DIV. 1211 GENEVA 23 SWITZERLAND		ABBREV: LUDS_CONNECTORS		AST_MODIFIED=Mon Sep 20 08:44:37 2004		
	DESSIN: DOMINIQUE GIGI			ETUDE:		DATE:	




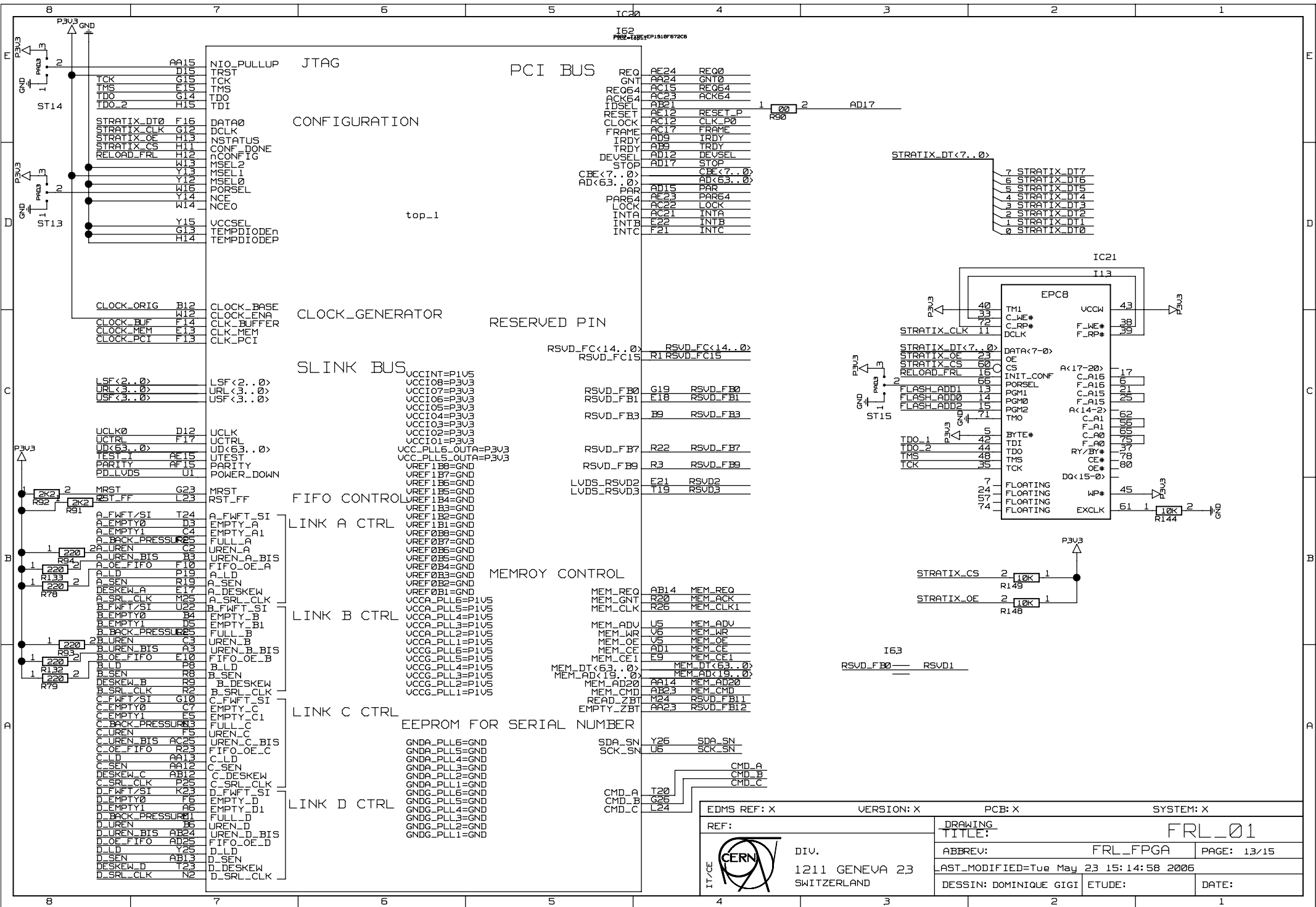
EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE:		FRL_01			
 DIV. 1211 GENEVA 23 SWITZERLAND		ABBREU: PCI_FOR_NIC		PAGE: 10/15			
		AST_MODIFIED: Mon Sep 20 08:44:28 2004		DESSIN: DOMINIQUE GIGI		ETUDE:	



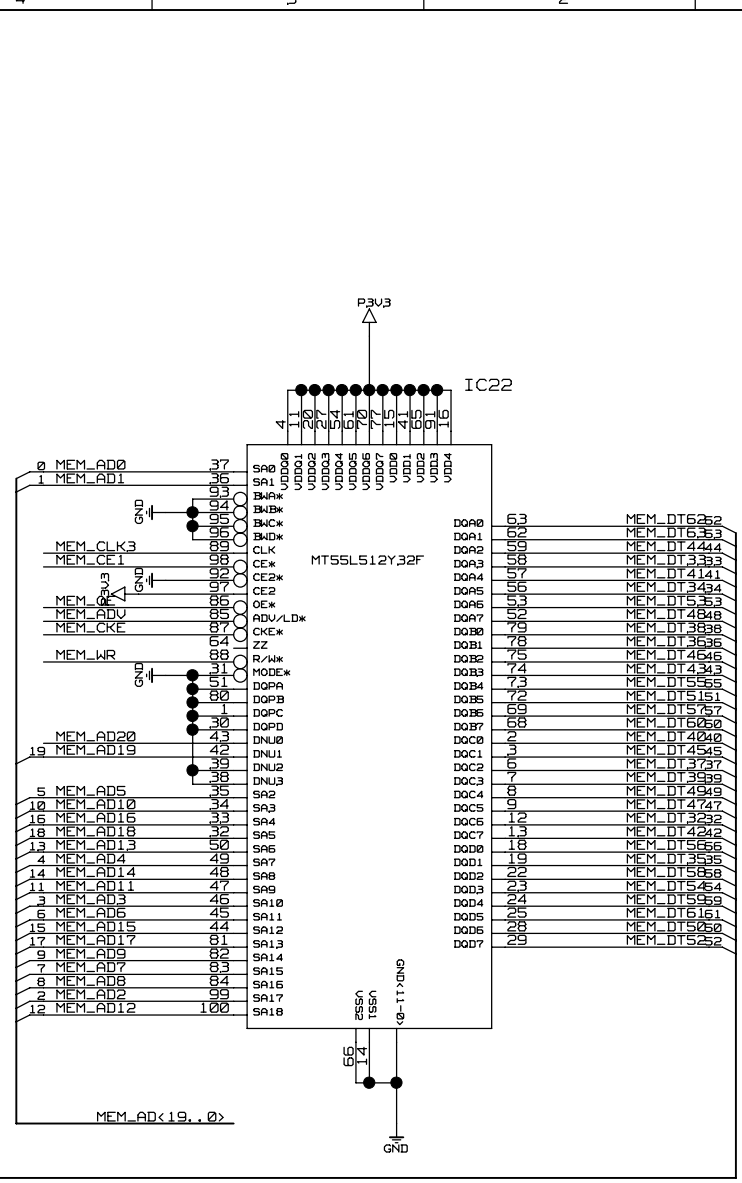
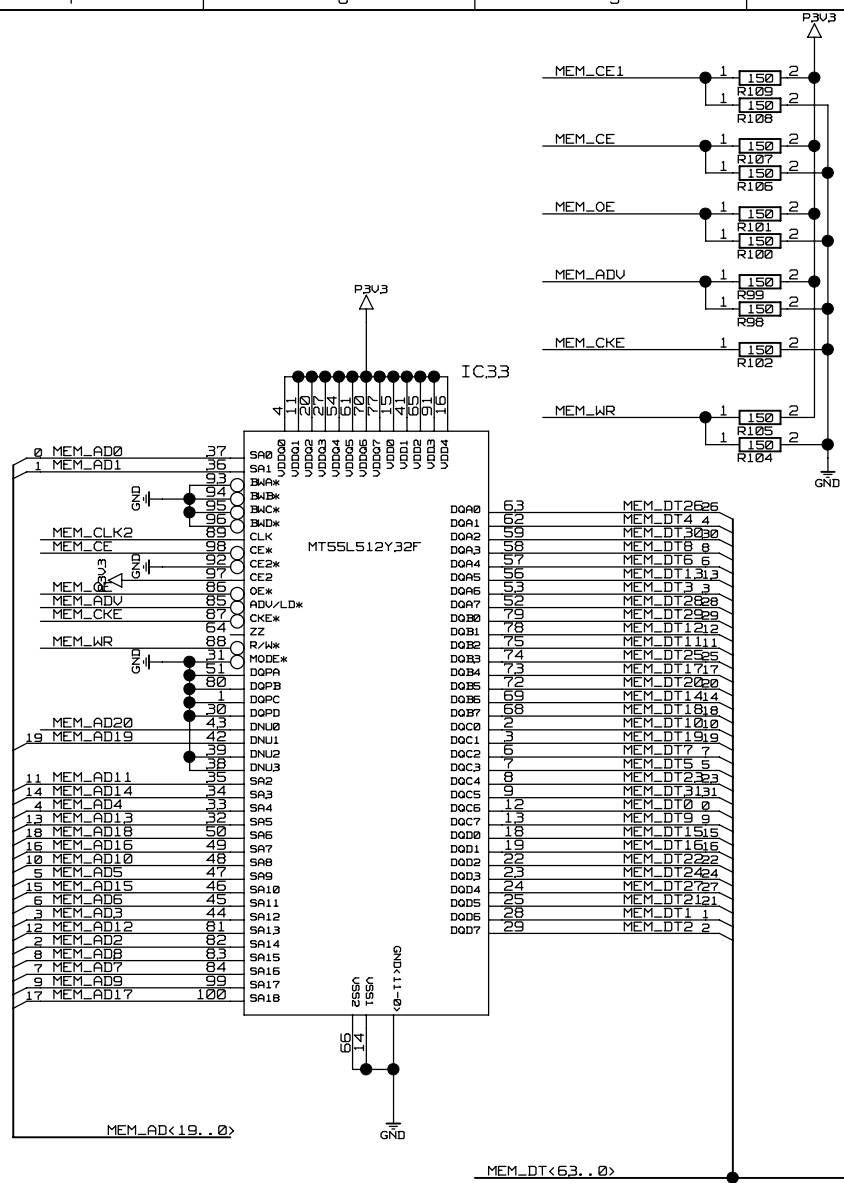
EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE: FRL_01		
 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: EXTENSION_CONNECTOR	PAGE: 11/15	
	LAST_MODIFIED=Mon Mar 13 17:39:35 2006		
	DESSIN: DOMINIQUE GIGI	ETUDE:	DATE:




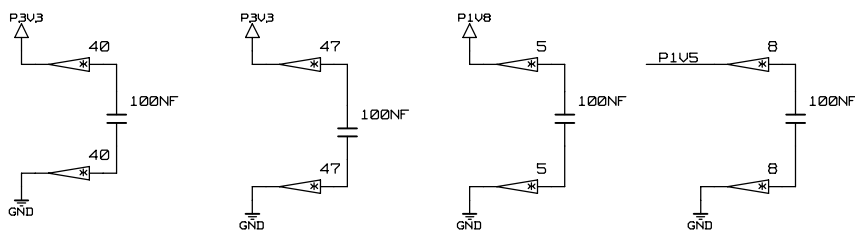
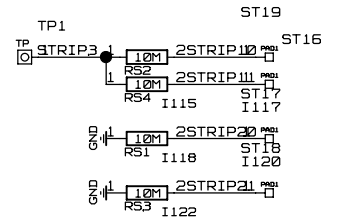
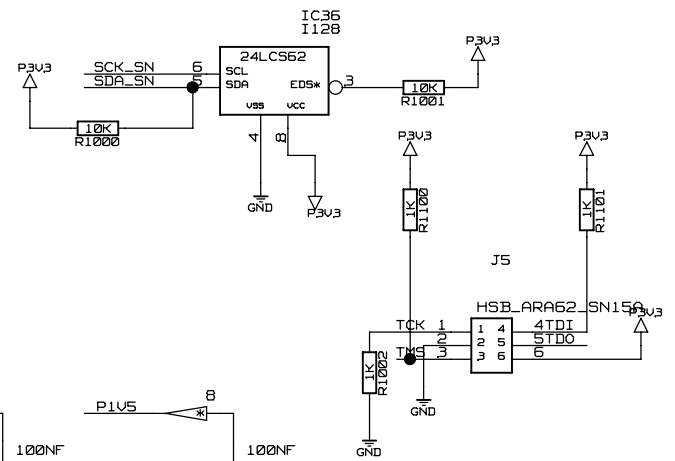
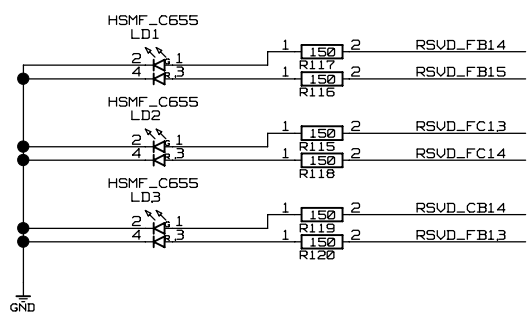
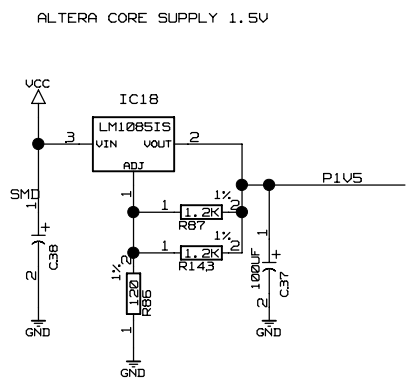
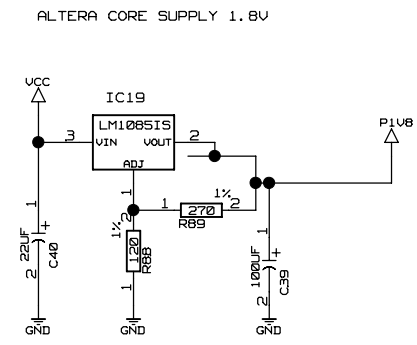
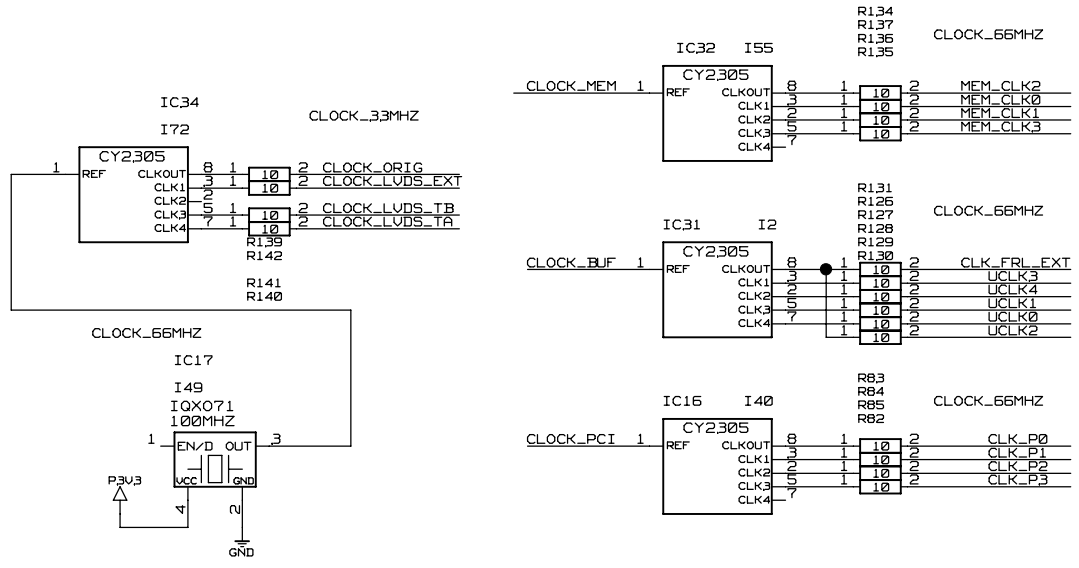
EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE: FRL_01		
 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREU: MEMORY_ZBT	PAGE: 12/15	
	LAST_MODIFIED=Mon Sep 20 08:44:29 2004		
DESSIN: DOMINIQUE GIGI		ETUDE:	DATE:



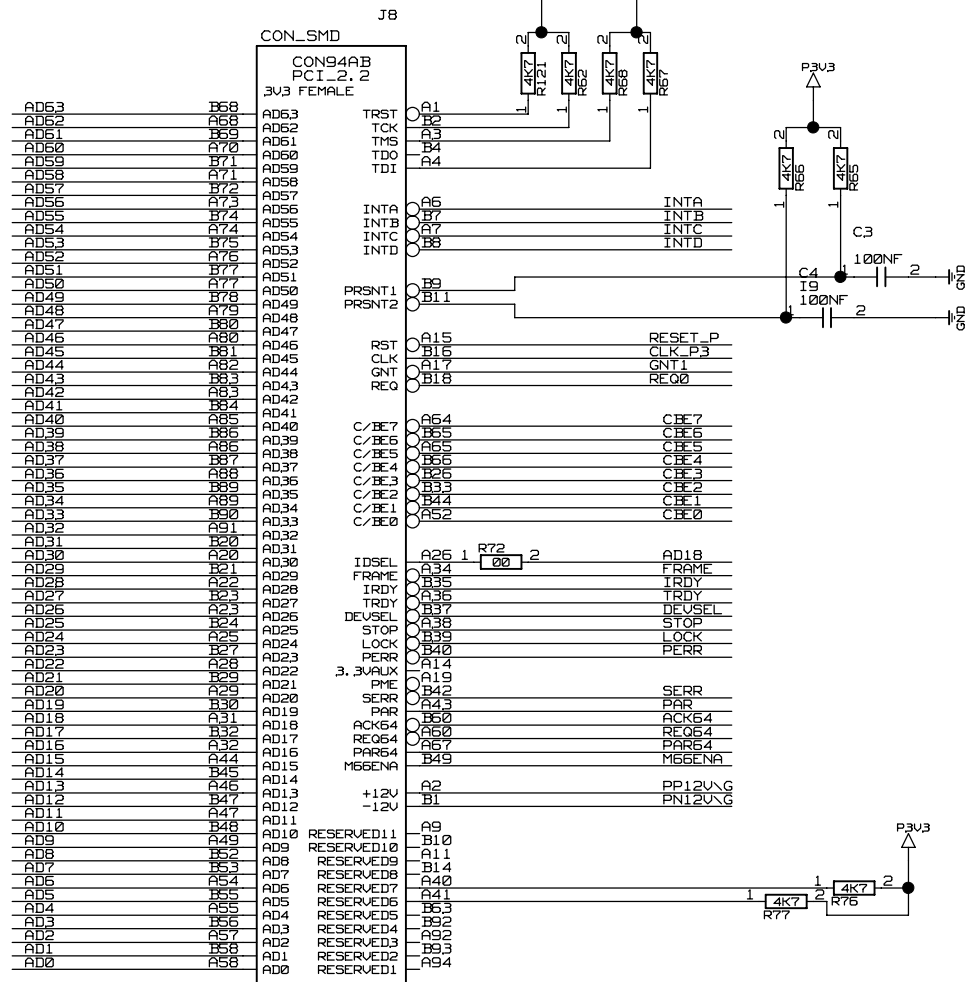
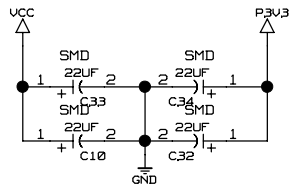
EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE:		FRL_01			
DIV.		ABBREV:		FRL_FPGA		PAGE: 13/15	
1211 GENEVA 23 SWITZERLAND		AST_MODIFIED=		Tue May 23 15:14:58 2006			
IT/CE		DESSIN: DOMINIQUE GIGI		ETUDE:		DATE:	




EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE:	FRL_01	
 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREU: MEMORY_ZBT	PAGE: 14/15	
	AST_MODIFIED=Mon Mar 13 15:09:37 2006		
	DESSIN: DOMINIQUE GIGI	ETUDE:	DATE:



EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE:		FRL_01			
IT/CE		DIV. 1211 GENEVA 23 SWITZERLAND		ABBREU: CLOCK_CONTROLLER		PAGE: 15/15	
				AST_MODIFIED: Tue Mar 14 10:04:07 2006			
				DESSIN: DOMINIQUE GIGI		ETUDE:	
						DATE:	



EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF:		DRAWING TITLE:		FRL_01			
 DIV. 1211 GENEVA 23 SWITZERLAND		ABBREU: PCI_DEBUG LAST_MODIFIED=Mon Sep 20 08:44:32 2004 DESSIN: DOMINIQUE GIGI		PAGE: ANNEXE ETUDE:		DATE:	