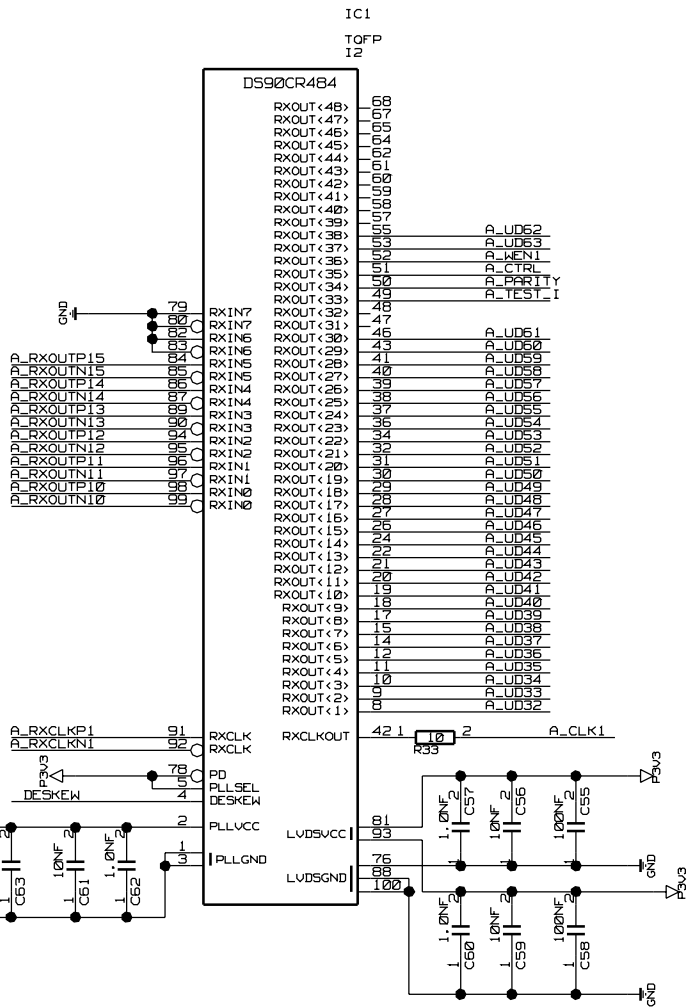
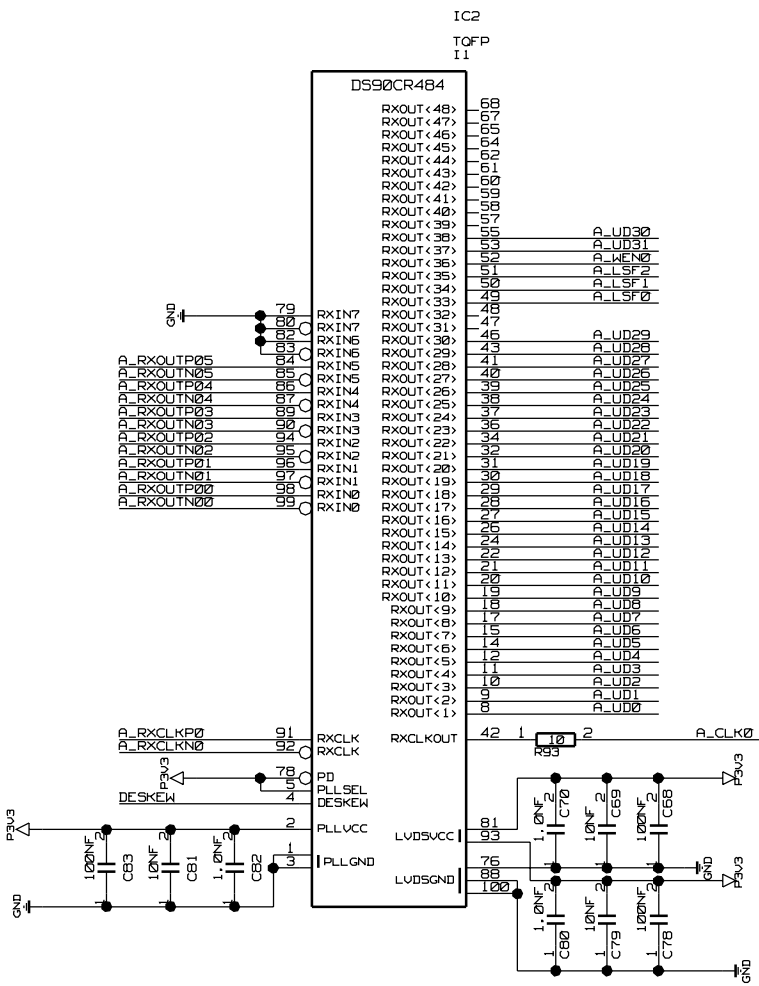
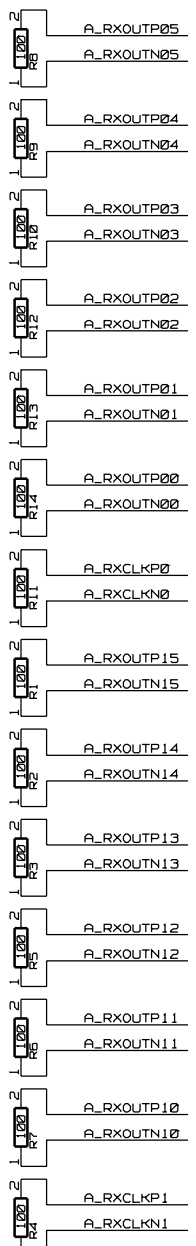

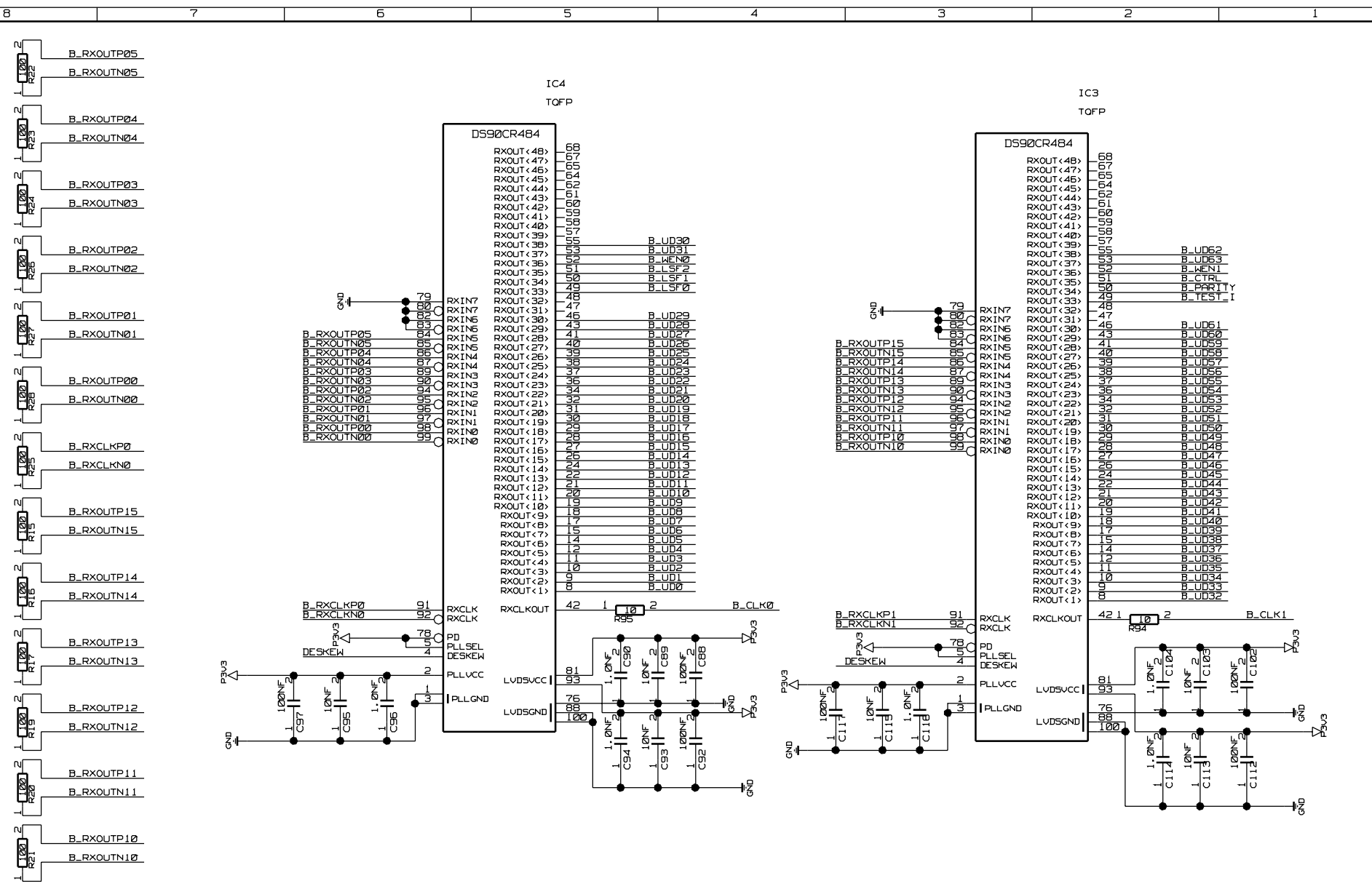



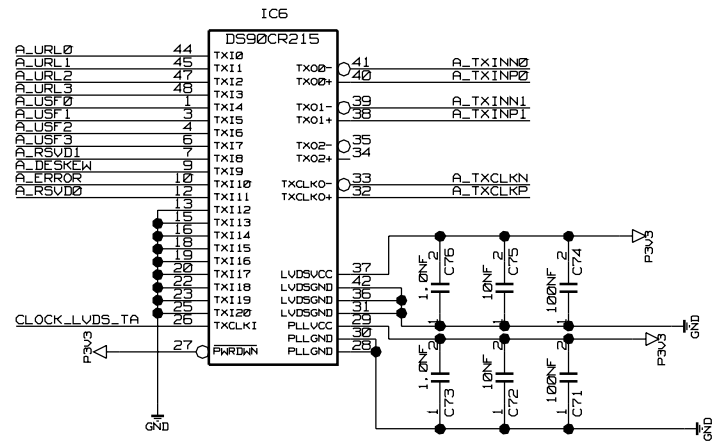
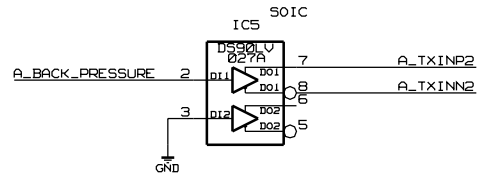
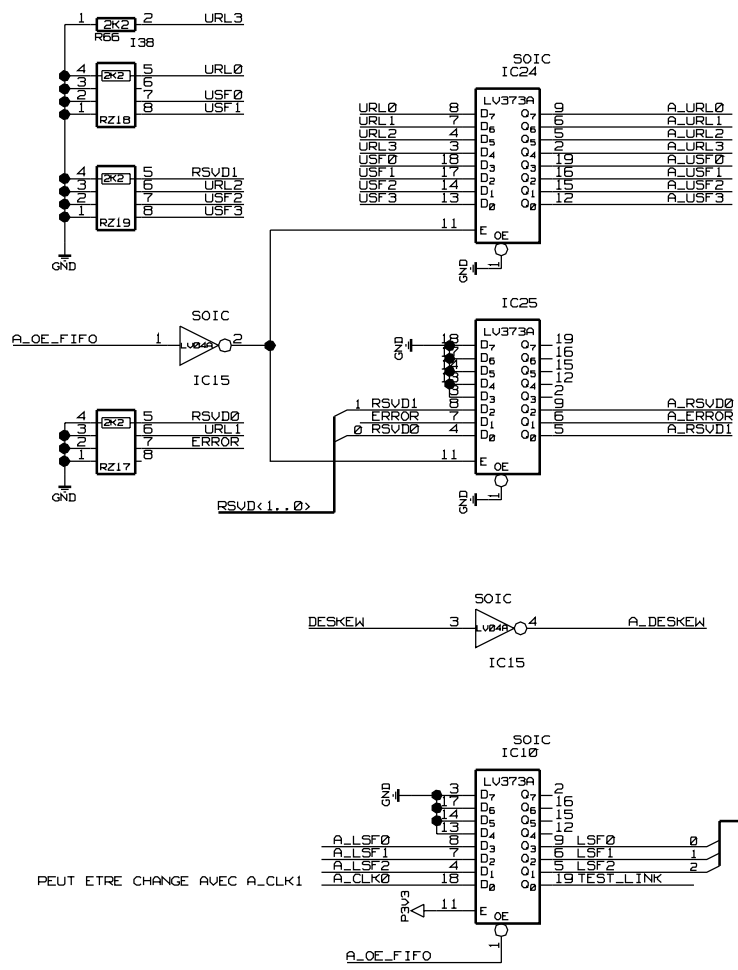
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	Div.	ABBREV: COMPACTPCI_CONNECTOR	PAGE: 1/15
	1211 GENEVA 23	-AST_MODIFIED= Tue Aug 19 16:42:14 2003	
	SWITZERLAND	DESSIN: DOMINIQUE GIGI	ETUDE: DATE:




EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE:		FRL_01
 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV:	LVDS_1_LINK_A	PAGE: 2/15
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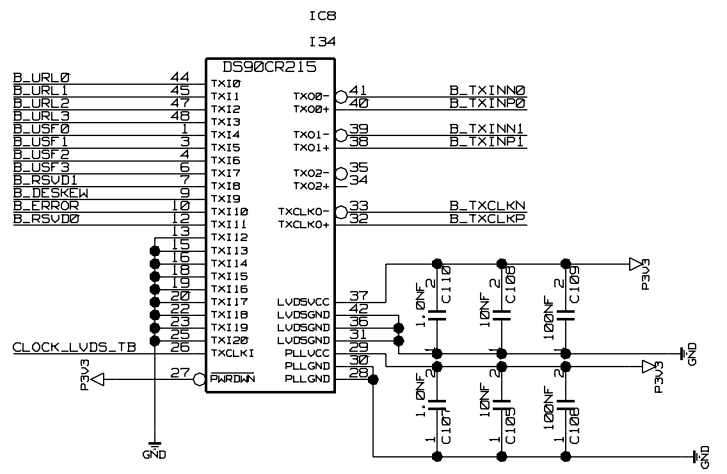
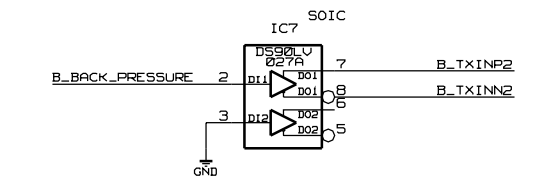
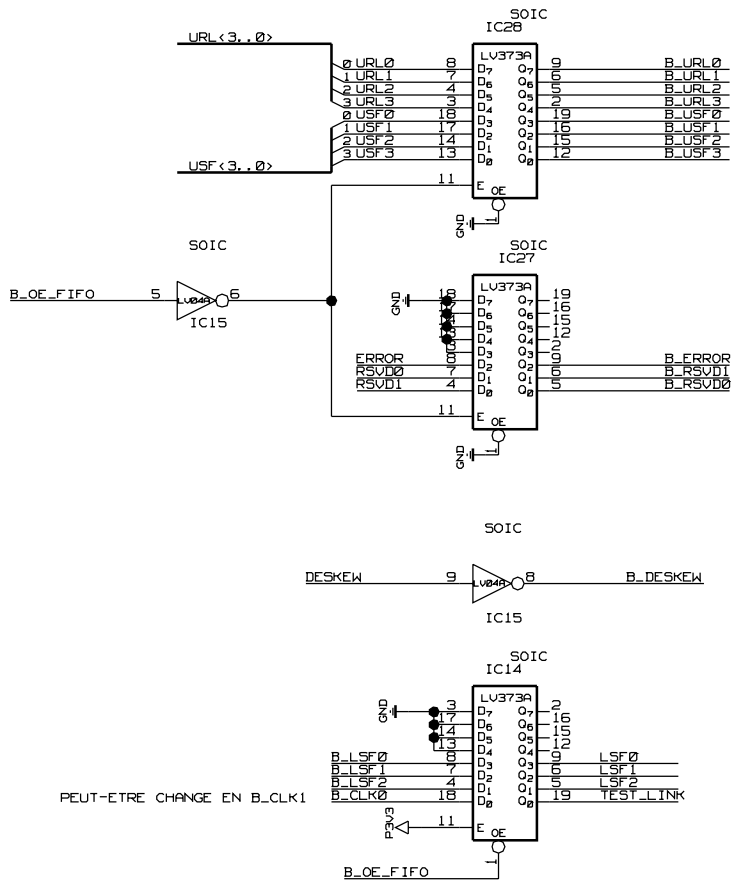



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 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREVI: LVDS_1_LINK_B	PAGE: 3/15	
	LAST_MODIFIED= Tue Aug 19 16:43:41 2003		
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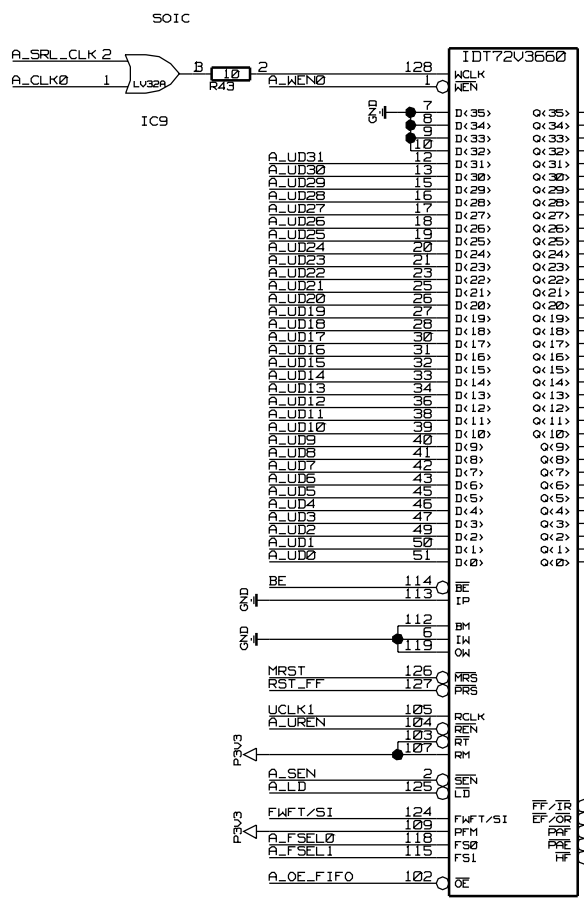


PEUT ETRE CHANGE AVEC A\_CLK1

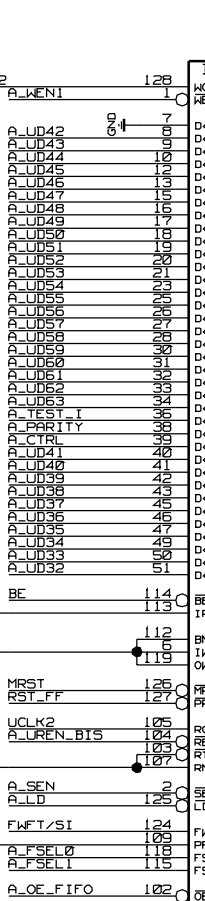
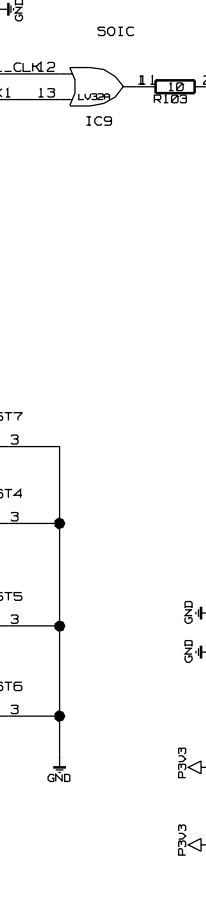
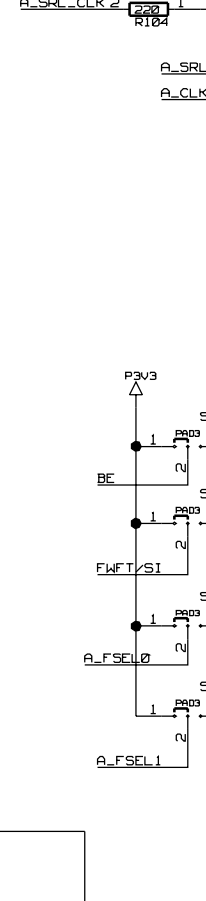
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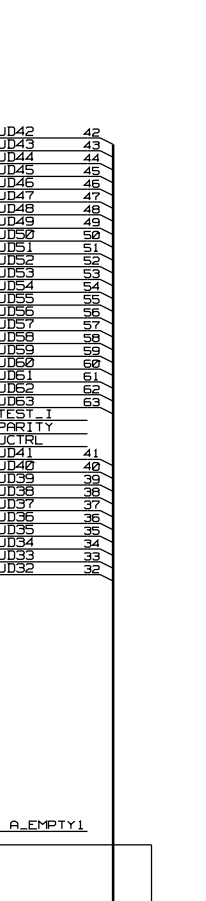
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 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREU: LVDS_2_LINK_B		LAST_MODIFIED= Tue Aug 19 16:45:05 2003
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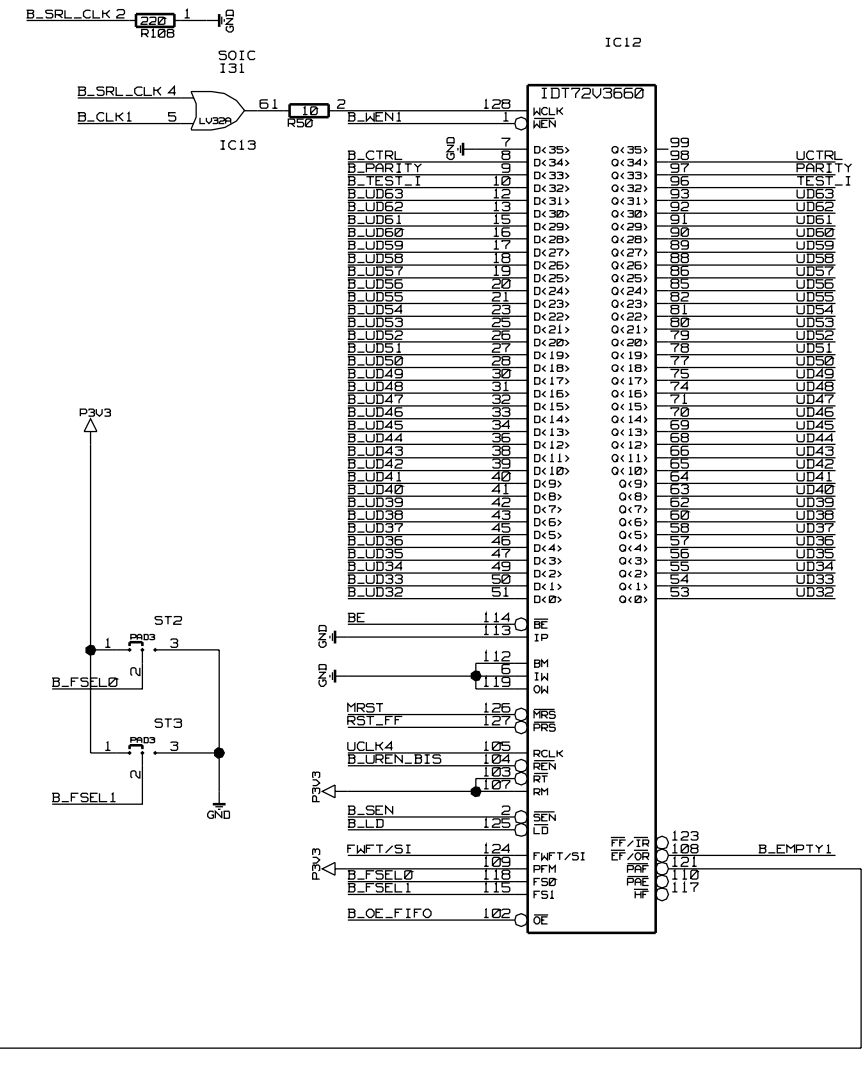
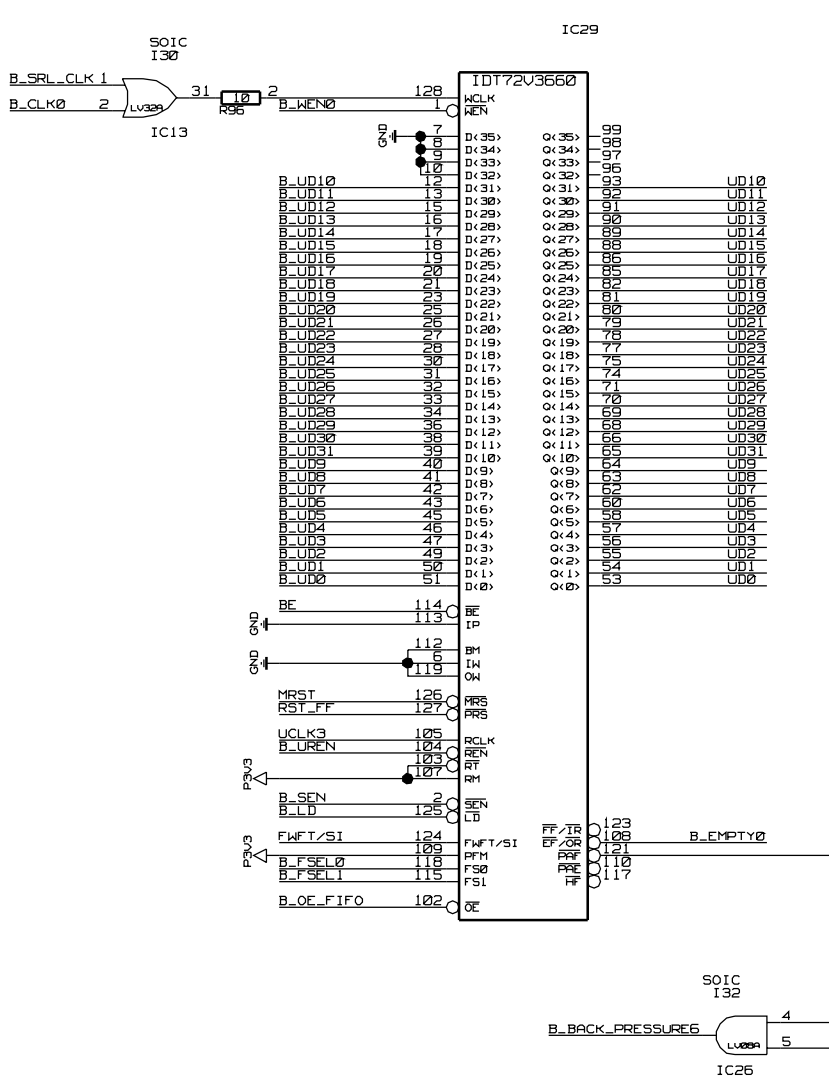
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UD29	29
UD28	28
UD27	27
UD26	26
UD25	25
UD24	24
UD23	23
UD22	22
UD21	21
UD20	20
UD19	19
UD18	18
UD17	17
UD16	16
UD15	15
UD14	14
UD13	13
UD12	12
UD11	11
UD10	10
UD9	9
UD8	8
UD7	7
UD6	6
UD5	5
UD4	4
UD3	3
UD2	2
UD1	1
UD0	0




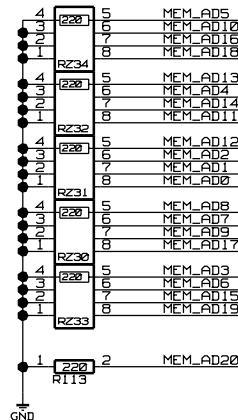
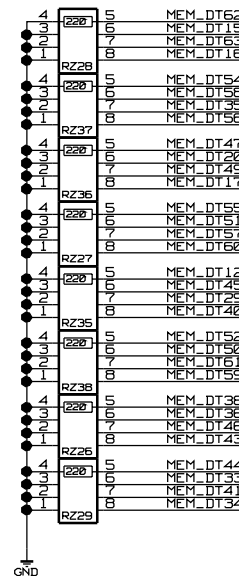
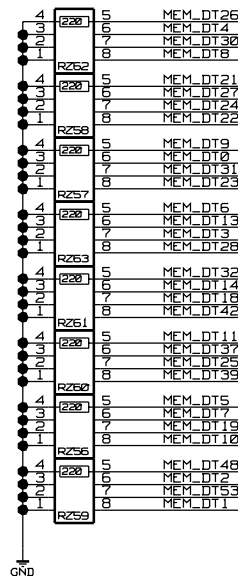
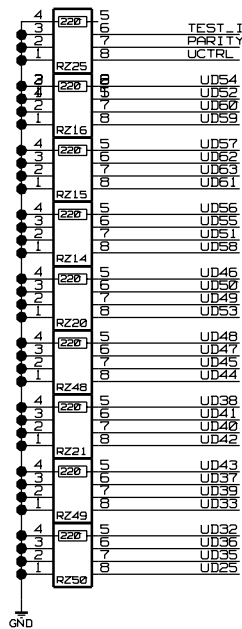
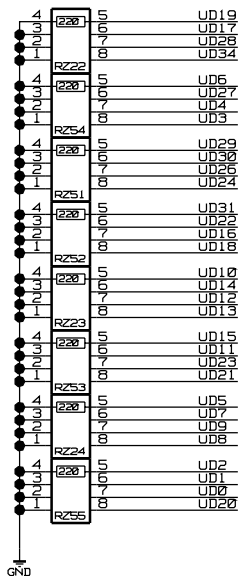
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UD41	41
UD40	40
UD39	39
UD38	38
UD37	37
UD36	36
UD35	35
UD34	34
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UD31	31
UD30	30
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UD28	28
UD27	27
UD26	26
UD25	25
UD24	24
UD23	23
UD22	22
UD21	21
UD20	20
UD19	19
UD18	18
UD17	17
UD16	16
UD15	15
UD14	14
UD13	13
UD12	12
UD11	11
UD10	10
UD9	9
UD8	8
UD7	7
UD6	6
UD5	5
UD4	4
UD3	3
UD2	2
UD1	1
UD0	0




EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE:		FRL_01
ABBREV: CERN		BUFFER_LINK_A	PAGE: 6/15
LAST_MODIFIED= Tue Aug 19 16:45:53 2003			
DESTINDOMINIQUE GIGI		ETUDE:	DATE:

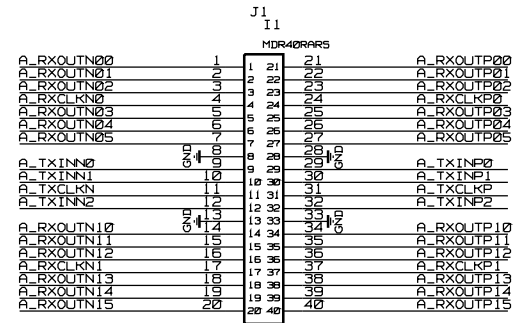
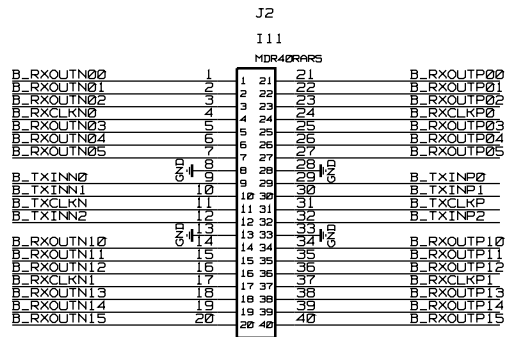



EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
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 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV:	BUFFER_LINK_B	PAGE: 7/15
	LAST_MODIFIED= Tue Aug 19 16:46:41 2003		
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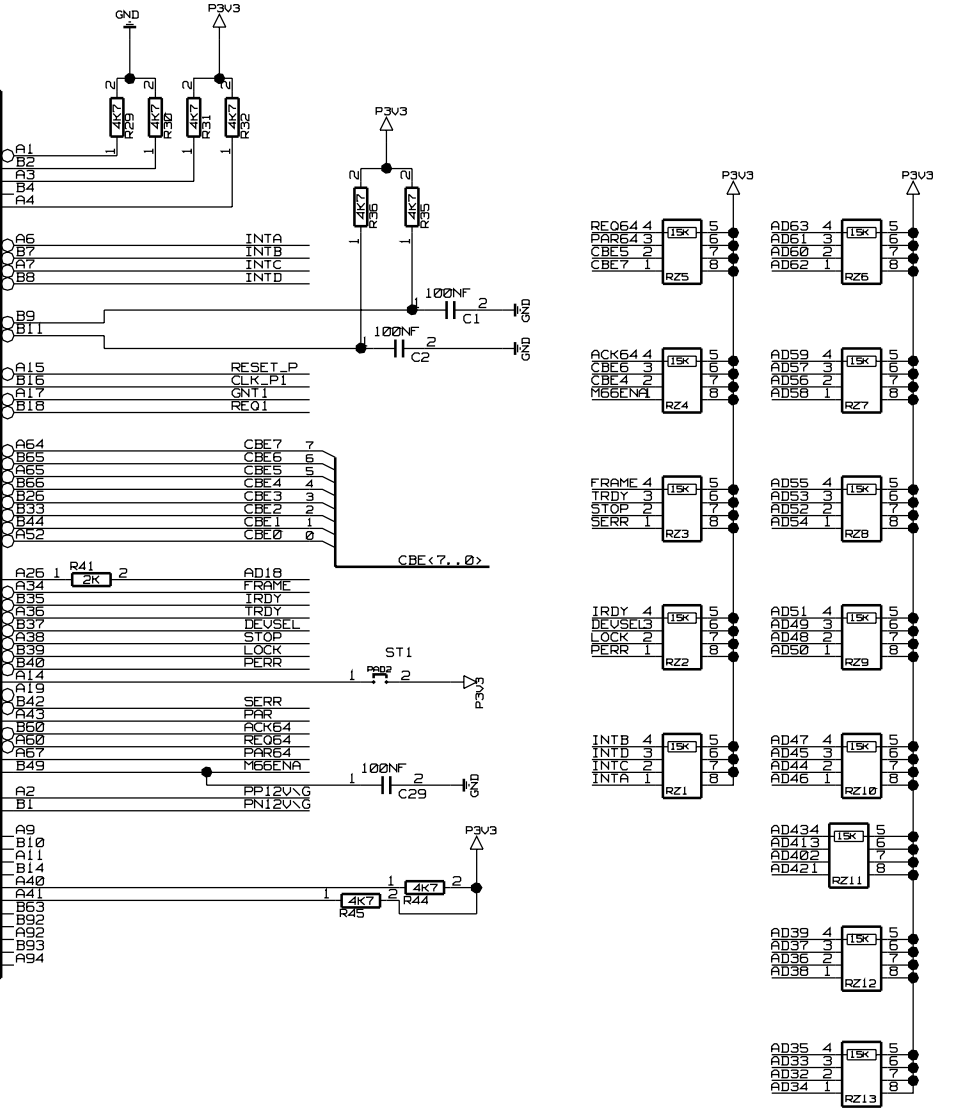
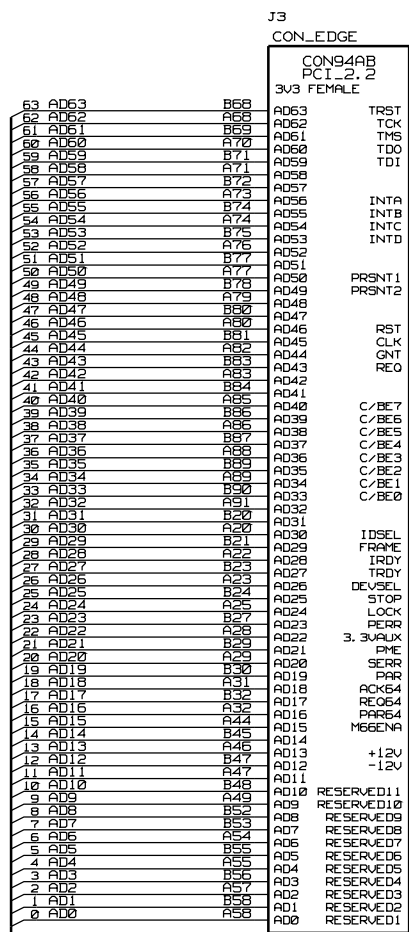
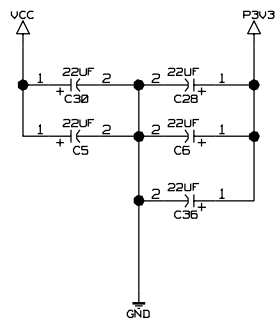


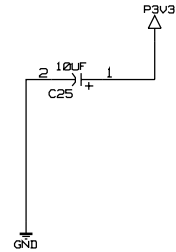
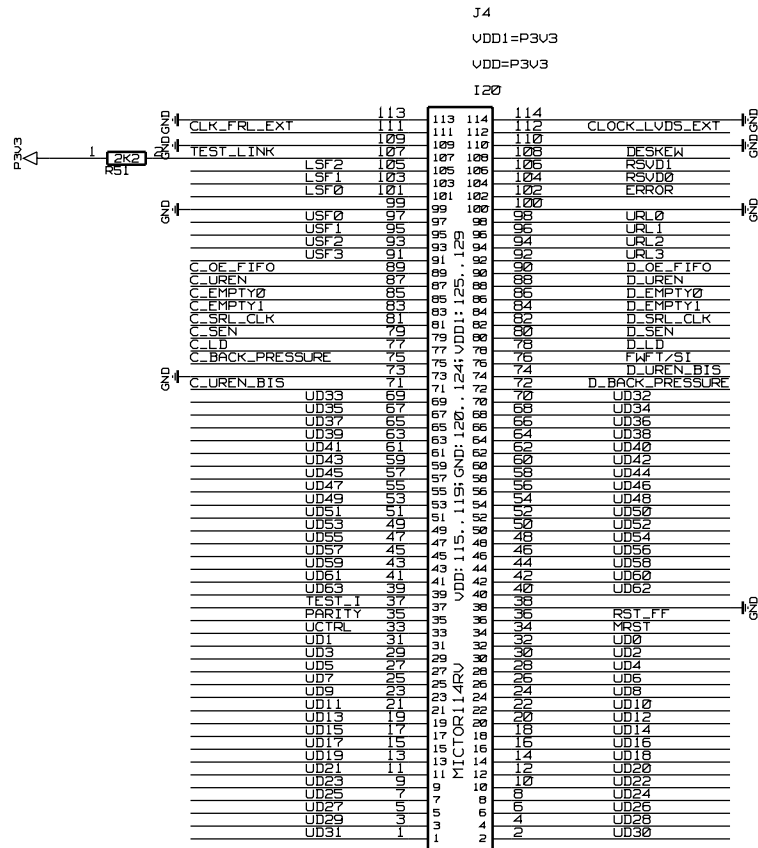
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 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: PULL_DOWN_NETWORK	PAGE: 8/15	
	LAST_MODIFIED= Tue Aug 19 16:47:28 2003		
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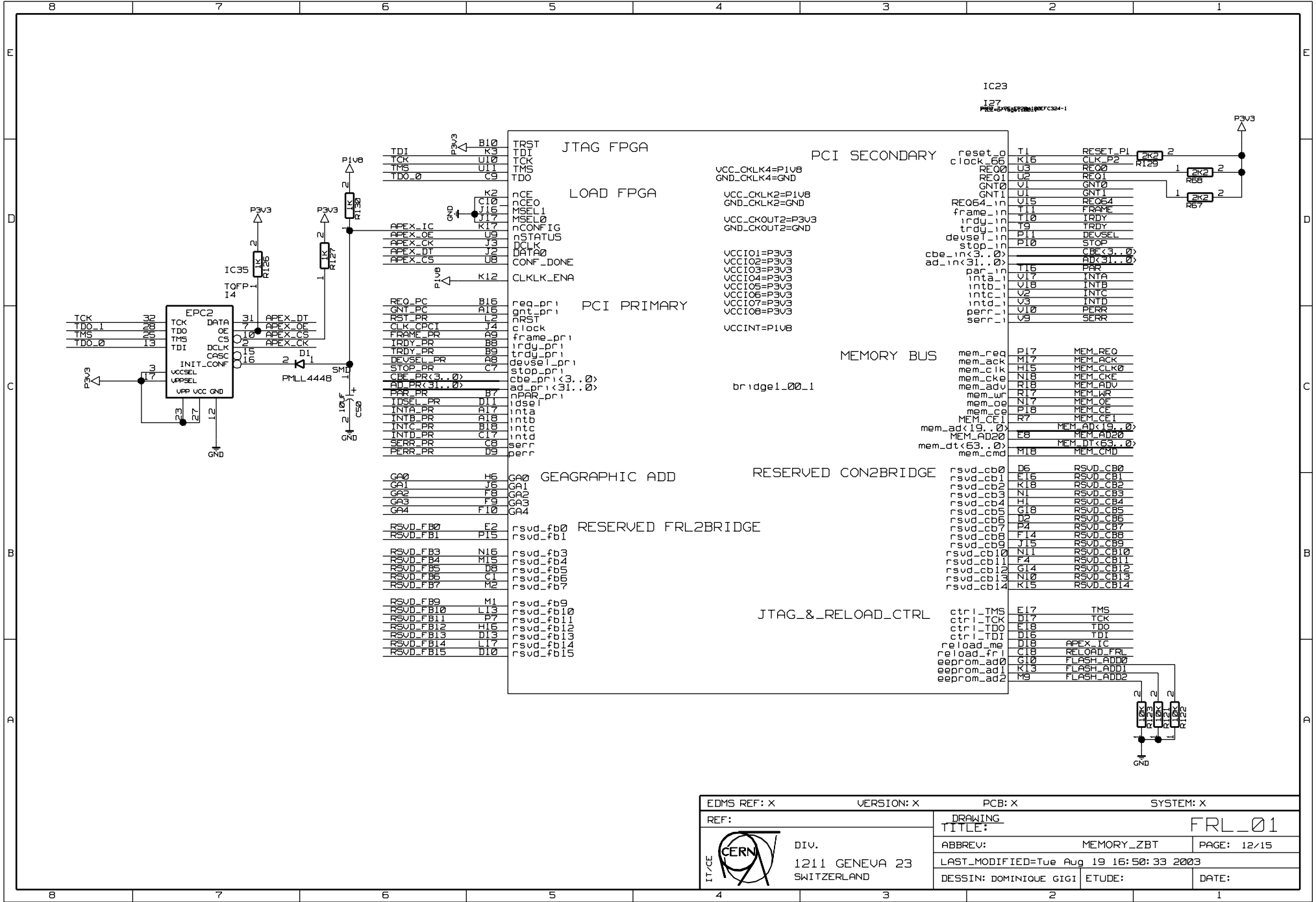


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 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREU: LVDS_CONNECTORS	PAGE: 9/15	
	LAST_MODIFIED= Tue Aug 19 16:48:14 2003		
	DESSIN: DOMINIQUE GIGI	ETUDE:	DATE:





EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE: FRL_01		
 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: EXTENSION_CONNECTOR	PAGE: 11/15	
	LAST_MODIFIED= Tue Aug 19 16:49:49 2003		
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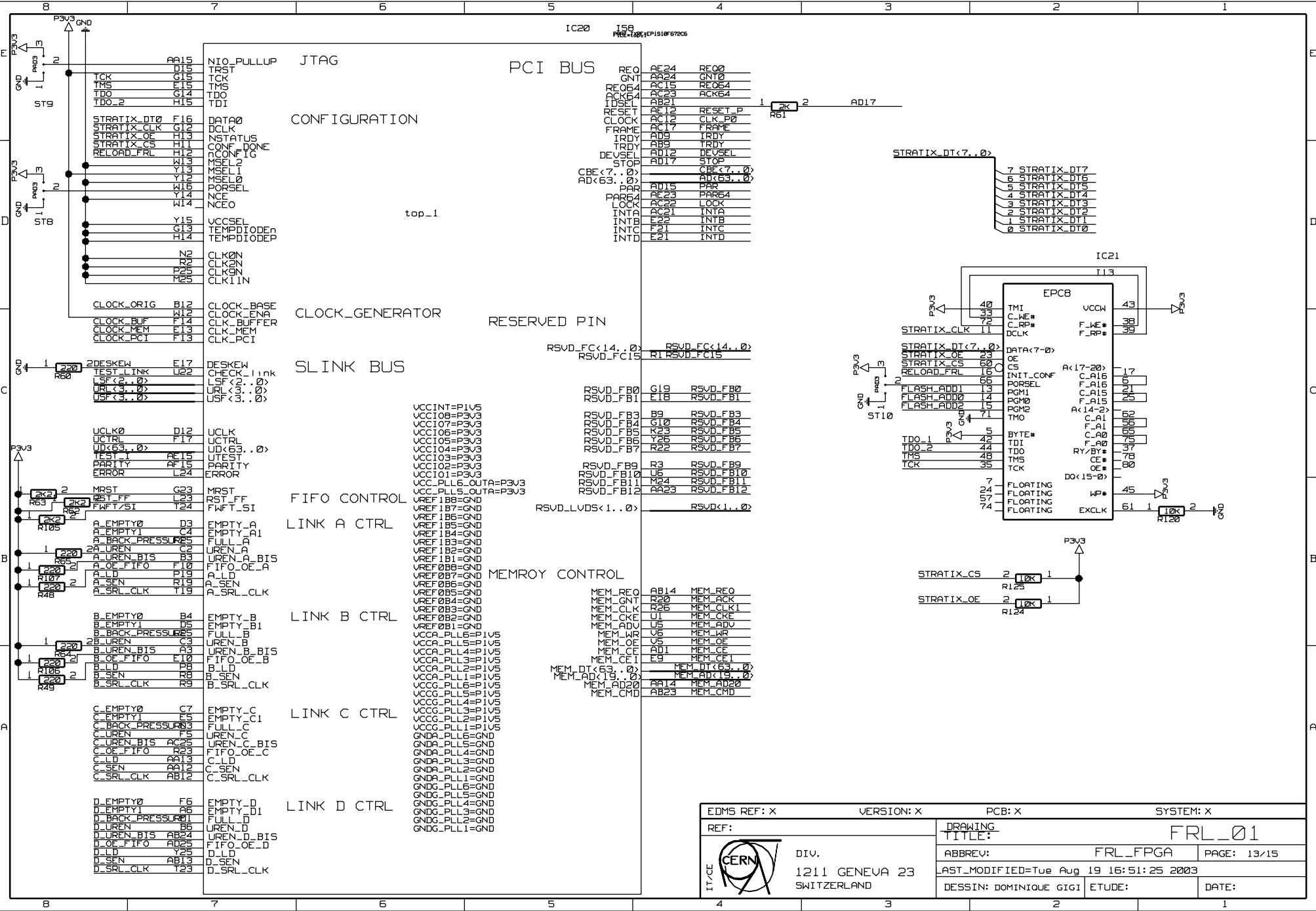
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 TCK K10  
 TMS U10  
 TDO\_C9  
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 APEX\_IC K12  
 APEX\_OE U9  
 APEX\_CK J3  
 APEX\_DT J1  
 APEX\_CS U8  
 REO\_PC B16  
 GNT\_PC A16  
 RST\_PR L2  
 CLK\_CPC1 J4  
 FRAME\_PR J4  
 IRDY\_PR BB  
 TRDY\_PR BB  
 DEVSEL\_PR AB  
 STOP\_PR C7  
 CBE\_PR<3..0>  
 AD\_PR<31..0>  
 PAR\_PR B7  
 IDSEL\_PR D11  
 INTA\_PR A17  
 INTB\_PR A18  
 INTC\_PR B18  
 INTD\_PR C17  
 SERR\_PR CB  
 PERR\_PR D9  
 CA0 H6  
 CA1 J0  
 CA2 F8  
 CA3 F9  
 CA4 F10  
 RSVD\_FB0 E2  
 RSVD\_FB1 P15  
 RSVD\_FB3 N16  
 RSVD\_FB4 M15  
 RSVD\_FB5 D6  
 RSVD\_FB6 G1  
 RSVD\_FB7 M2  
 RSVD\_FB9 M1  
 RSVD\_FB10 L7  
 RSVD\_FB11 P7  
 RSVD\_FB12 H16  
 RSVD\_FB13 D13  
 RSVD\_FB14 L17  
 RSVD\_FB15 D10  
 TRST  
 TDI  
 TCK  
 TMS  
 TDO  
 nCE  
 nCEO  
 MSEL1  
 MSEL0  
 nCONFIG  
 nSTATUS  
 DCLK  
 DATA0  
 CONF\_DONE  
 CLKLK\_ENA  
 req\_pr1  
 gnt\_pr1  
 nRST  
 clock  
 frame\_pr1  
 irdy\_pr1  
 trdy\_pr1  
 devsel\_pr1  
 stop\_pr1  
 cbe\_pr1<3..0>  
 ad\_pr1<31..0>  
 idsel1  
 inta  
 intb  
 intc  
 intd  
 serr  
 perr  
 rsvd\_fb0  
 rsvd\_fb1  
 rsvd\_fb3  
 rsvd\_fb4  
 rsvd\_fb5  
 rsvd\_fb6  
 rsvd\_fb7  
 rsvd\_fb9  
 rsvd\_fb10  
 rsvd\_fb11  
 rsvd\_fb12  
 rsvd\_fb13  
 rsvd\_fb14  
 rsvd\_fb15


**JTAG FPGA**  
**LOAD FPGA**  
**PCI PRIMARY**  
**RESERVED CON2BRIDGE**  
**RESERVED FRL2BRIDGE**  
**JTAG\_&\_RELOAD\_CTRL**

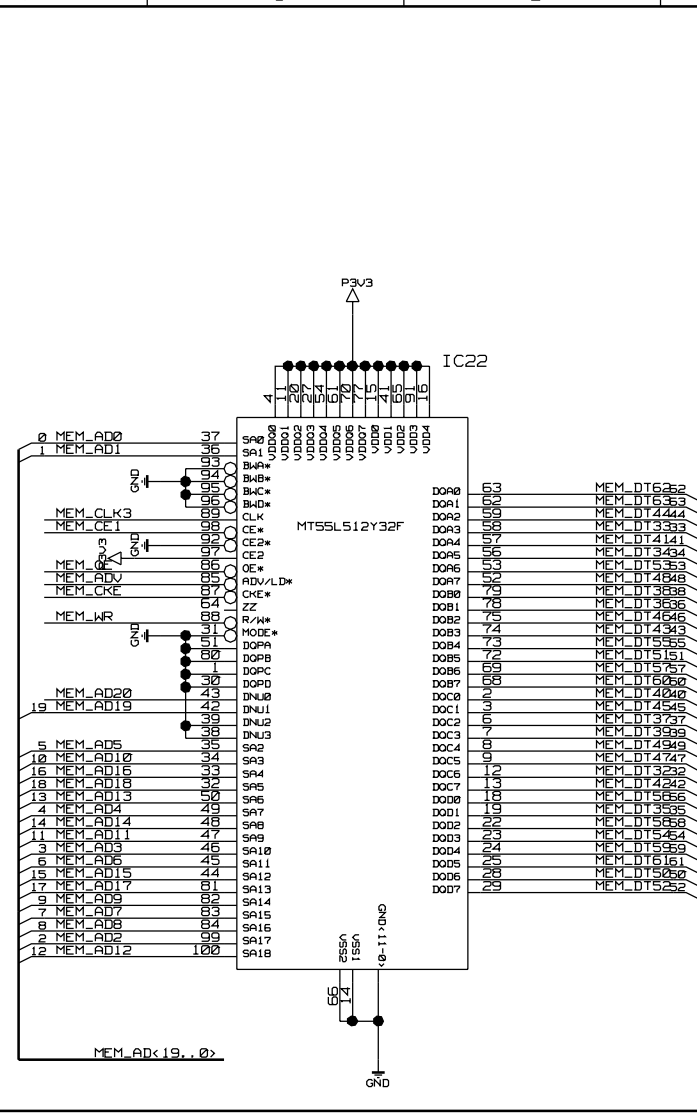
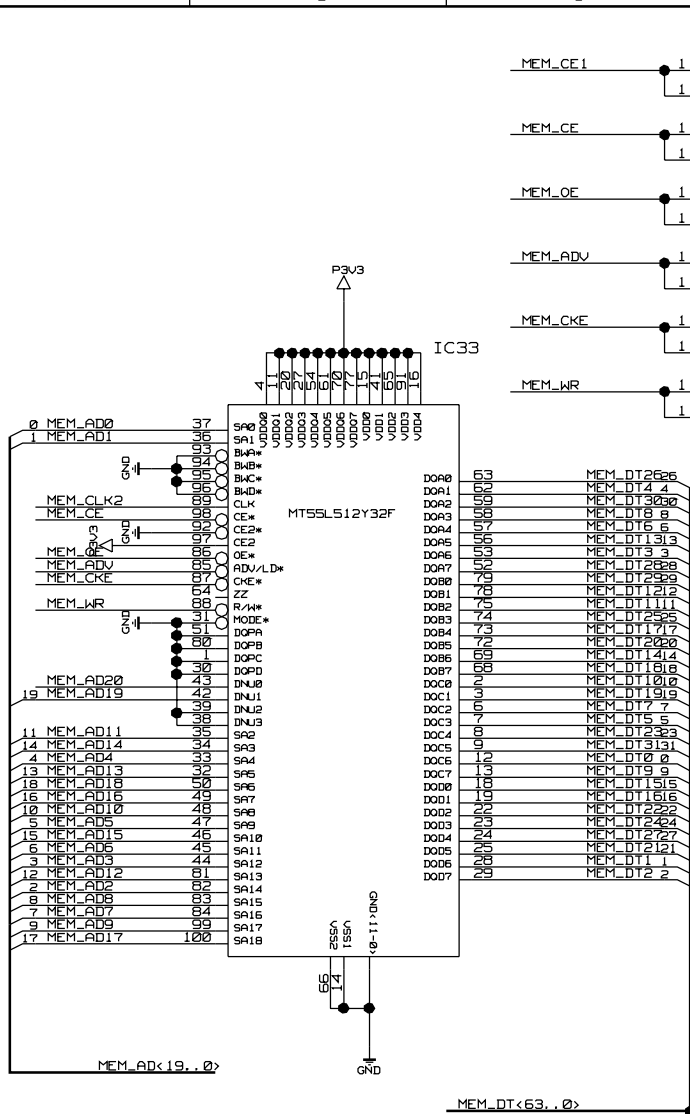
**PCI SECONDARY**  
 reset\_0  
 clock\_66  
 REO0  
 REO1  
 GNT0  
 GNT1  
 REO54\_in  
 frame\_in  
 irdy\_in  
 trdy\_in  
 devsel\_in  
 stop\_in  
 cbe\_in<3..0>  
 ad\_in<31..0>  
 par\_in  
 inta\_in  
 intb\_in  
 intc\_in  
 intd\_in  
 perr\_in  
 serr\_in  
 VCC\_CLK4=P1V8  
 GND\_CLK4=GND  
 VCC\_CLK2=P1V8  
 GND\_CLK2=GND  
 VCC\_CKOUT2=P3V3  
 GND\_CKOUT2=GND  
 VCCI01=P3V3  
 VCCI02=P3V3  
 VCCI03=P3V3  
 VCCI04=P3V3  
 VCCI05=P3V3  
 VCCI06=P3V3  
 VCCI07=P3V3  
 VCCI08=P3V3  
 VCCINT=P1V8  
 mem\_req  
 mem\_ack  
 mem\_clk  
 mem\_cke  
 mem\_adv  
 mem\_wr  
 mem\_or  
 mem\_ce  
 MEM\_CE1  
 mem\_ad<19..0>  
 MEM\_AD20  
 mem\_dt<63..0>  
 mem\_cmd  
 rsvd\_cb0  
 rsvd\_cb1  
 rsvd\_cb2  
 rsvd\_cb3  
 rsvd\_cb4  
 rsvd\_cb5  
 rsvd\_cb6  
 rsvd\_cb7  
 rsvd\_cb8  
 rsvd\_cb9  
 rsvd\_cb10  
 rsvd\_cb11  
 rsvd\_cb12  
 rsvd\_cb13  
 rsvd\_cb14  
 ctrl\_TMS  
 ctrl\_TCK  
 ctrl\_TDO  
 ctrl\_TDI  
 reload\_ma  
 reload\_fr1  
 eeprom\_ad0  
 eeprom\_ad1  
 eeprom\_ad2


**MEMORY BUS**  
**IC23**  
**IC27**  
 T1  
 CLK\_P2  
 REO0  
 REO1  
 GNT0  
 GNT1  
 REO54  
 FRAME  
 TRDY  
 TRDY  
 DEVSEL  
 STOP  
 CBE<3..0>  
 AD<31..0>  
 PAR  
 INTA  
 INTB  
 INTC  
 INTD  
 PERR  
 SERR  
 MEM\_RE0  
 MEM\_ACK  
 MEM\_CLK0  
 MEM\_KE  
 MEM\_ADV  
 MEM\_WR  
 MEM\_OR  
 MEM\_CE  
 MEM\_CE1  
 MEM\_AD<19..0>  
 MEM\_AD20  
 MEM\_DT<63..0>  
 MEM\_CMD  
 RSVD\_CB0  
 RSVD\_CB1  
 RSVD\_CB2  
 RSVD\_CB3  
 RSVD\_CB4  
 RSVD\_CB5  
 RSVD\_CB6  
 RSVD\_CB7  
 RSVD\_CB8  
 RSVD\_CB9  
 RSVD\_CB10  
 RSVD\_CB11  
 RSVD\_CB12  
 RSVD\_CB13  
 RSVD\_CB14  
 TMS  
 TCK  
 TDO  
 TDI  
 APEX\_IC  
 RELOAD\_FR1  
 FLASH\_ADD0  
 FLASH\_ADD1  
 FLASH\_ADD2

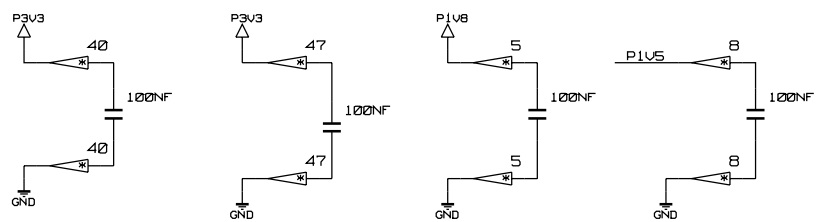
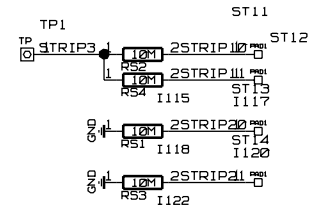
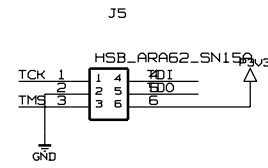
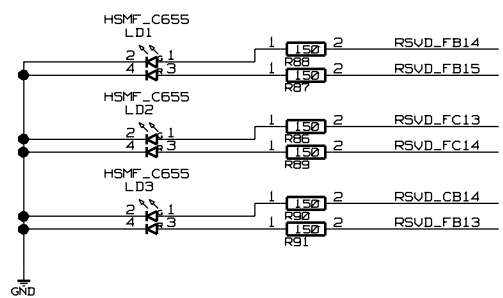
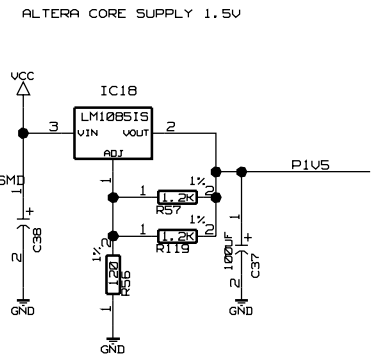
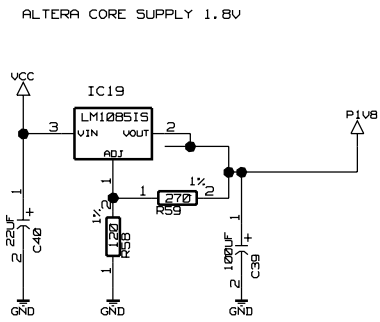
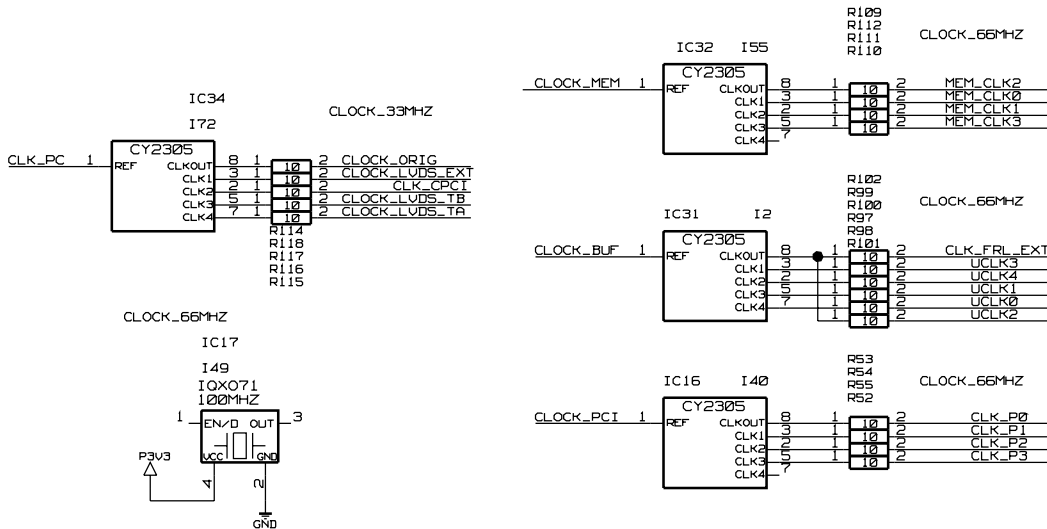
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	LAST_MODIFIED=Tue Aug 19 16:50:33 2003		
	DESSIN: DOMINIQUE GIGI	ETUDE:	DATE:



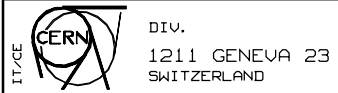
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	-AST_MODIFIED= Tue Aug 19 16:51:25 2003		
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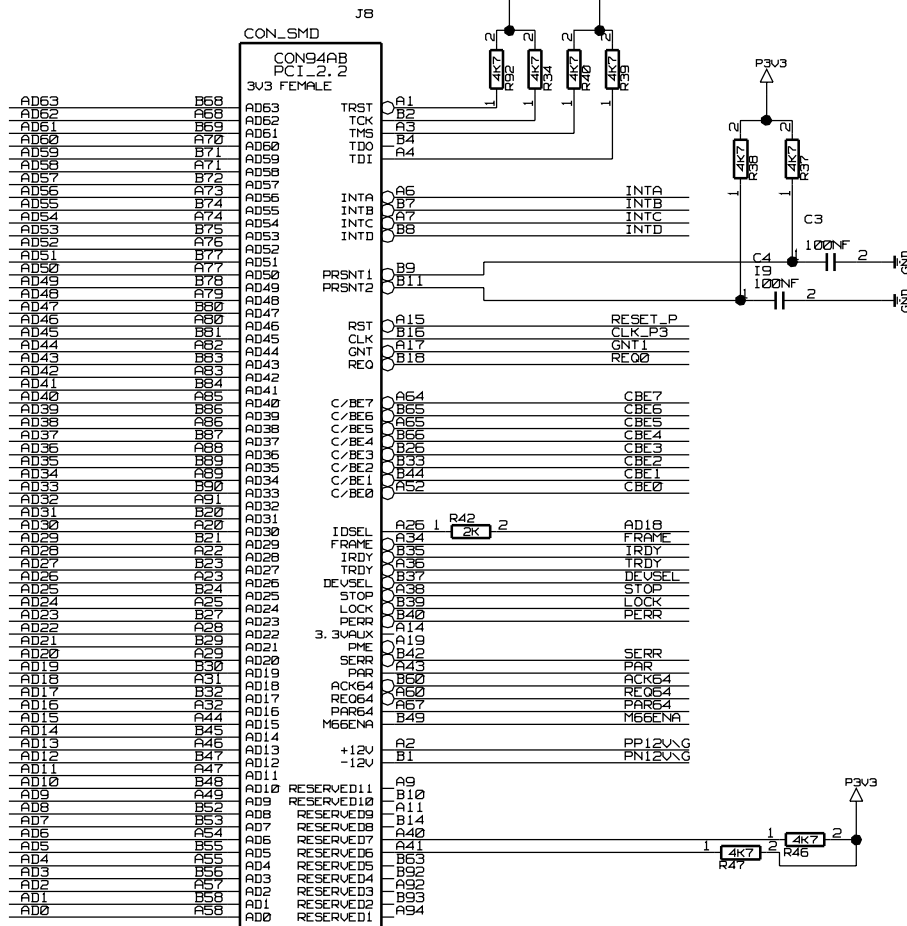
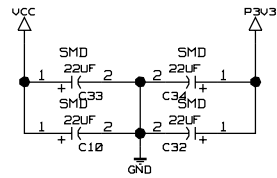



EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
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 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREVIATION: MEMORY_ZBT		PAGE: 14/15
	LAST MODIFIED= Tue Aug 19 16:52:21 2003		
	DESSIN: DOMINIQUE GIGI	ETUDE:	DATE:



EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE: FRL_01		PAGE: 15/15
ABBREV: CLOCK_CONTROLLER		AST_MODIFIED= Tue Aug 19 16:53:12 2003	
DESSIN: DOMINIQUE GIGI		ETUDE:	DATE:





EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF:	DRAWING TITLE: FRL_01		PAGE: ANNEXE
 DIV. 1211 GENEVA 23 SWITZERLAND	ABBREUV: PCI_DEBUG		LAST_MODIFIED=Tue Aug 19 16:53:48 2003
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	DATE:		