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FRL (FED Read-out Link)

(User manuel ver 5.00)

1 Introduction

The FRL (FED Read-out Link) is the first element of the Data Acquisition for CMS. It has two functions: it

-It moves data out of FEDs and push them to the first stage of the FED builder through a NIC card.

-It merges 2 to 4 events fragments coming from two to four FEDs (see figure 1), to be seen as one event fragment by the link. It feature has the advantage to increase the using of the bandwidth.

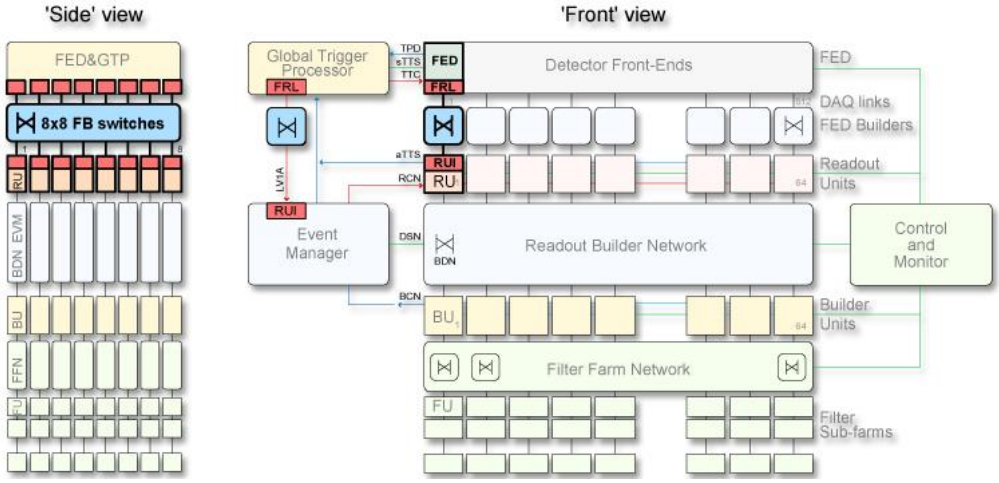

Figure 1: CMS Data Acquisition System

The total number of this board is 512. They will collect events fragments coming from more or less 650 FED's.

2 Description

The FRL is composed by three elements

- One CMC transmitter (Common Mezzanine Card)
- One cable (5, 10 or 15 meters)
- One CompactPCI board (the FRL itself)

The protocol used to transfer data from FED to the FRL is the Slink64 [1]. The media is the LVDS technology through a copper cable.

2.1 CMC transmitter

The CMC board (74 mm x 114 mm) will be plugged on the FED. It receives events form FED with the Slink64 protocol through 2 connectors (description annex A). The bandwidth is 64-bit data word @ max. 100 MHz.

On board, a FPGA (EP10K30QC208-2) has multiple functions:

- generates data according the event format, to test the link without controls form the FED (test mode).
- converts the data frequency (on connectors) to a frequency adapted for the cable length (5 meters 80 MHz, 10 meters 60 MHz, 15 meters 40 MHz).
-data is transferred on a LVDS technology with a multiplexing of 8 to minimize the numbers of copper conductors.

Figure 2 : CMC transmitter board

Some switches are mounted on board to choose the frequency (SW1, SW3) on the cable and a LVDS voltage (SW2). Those values will be set according the cable length (annex B).

2.2 Cable

The cable is an 18 pairs of wires twisted and shielded. The characteristics are 100 ohms differential impedance and the skew is 600 ps between pairs. It's actually a 3M Company cable with a MDR connector. The Amphenol Company has promise to continue to provide us prototypes.

2.3 FRL CompactPCI board

The FRL 6U CompactPCI board is the main element of the subject. This board is composed of two PCI bus:

- The host is a CompactPCI bus of 32-bit @ 33MHz. It is used for control and for an optional way for the DAQ acquisition.
- The second PCI bus is internal of the board. It is a PCI bus 64-bit @ 66 MHz (a future use should be 64-bit @ 100 MHz PCI-x protocol).

The internal bus is connected to three elements: the bridge to access to and from the CompactPCI bus, the FRL function (a FPGA STRATIX ALTERA) and a straddle PCI connector 64-bit data width.
A ghost PCI connector at the back of the FRL is mounted on board used for the debugging.
A hole is done on board to accept a PCI board (NIC card) that will be plugged in the straddle PCI connector (see figure 3).

Figure 3 : FRL CompactPCI board

The board has two connectors on the front to receive data from up to two FEDs through the CMC transmitter and cable. Following these connector there are the LVDS receiver and a FIFO able to buffer 64 Kbytes of data. These FIFO is read by the FRL function (FPGA STRATIX).
The last component on board is a memory (4Mbytes) that can be used for multiple purposes (Spy mode, CPU code…). Its bandwidth is 800 Mbytes/s (64-bit up to 100MHz) shared between the FRL FPGA and the bridge (see applications below).

The block diagram of the board is shown figure 4.You can distinguish the three parts of the board: the internal PCI bus, the input of the board (LVDS), the memory.
The board is plugged in a Compact PCI crate controlled by a PC.

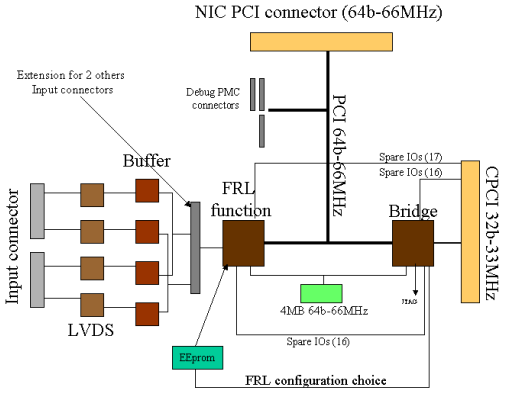

Figure 4 : FRL block diagram

The FRL is seen as an element with three functions:
-Bridge
-FRL logic
-Optical link Card (NIC card)

Each element is controlled independently one of the other. The bridge is not a real PCI to PCI Bridge. This option was abandoned where we see that most BIOS do not control correctly the memory allocation through PCI to PCI Bridge. It keeps the name 'Bridge' but not the function.
It acts as a PCI element where all thee FRL PCI elements are seen. It has also the PSY mode function and the access to the 4 Mbytes of memory.

The STRATIX FPGA is coupled with a flash memory that keeps firmwares. This flash memory can record up to four designs. Actually the four designs are assigned:
0: normal operation
1: to test the Myrinet functionality
2: Stand alone mode (data are produced in the FRL and send in the DAQ system.
3: Design to test the backplane trigger and backpressure

3 Functionality

The FRL is a CompactPCI board with 2 LVDS SLINK input on the front panel, a CompactPCI connector at the back and a NIC card plugged including an optical fiber connection.

The CompactPCI connection is used to control the board by a PC. The PC can setup the board, monitor it and receive event (PSY mode) for some analysis.
The CompactPCI is a 32 bit 33 MHz bus that is shared with maximum 16 FRLs.
The PC can access any registers of any elements of the FRL (FRL logic, bridge/spy function and NIC card).

The main function of the FRL is to receive events (Header-Payload-Trailer) from 1 or both input link (SLINK) in the front panel. Events come from FED on which a SLINK mezzanine card is plugged. A LVDS cable (6.5, 8, 10 or 11,5 meters) does the connection between SLINK mezzanine and one input link (0 or 1).
The SLINK mezzanine is a card that receives data from FED. The data is written to the card with a frequency given by the FED (up to 100MHz). The protocol used looks like a FIFO protocol. A backpressure indicates to the FED that DAQ is still able to ingurgitate some data word (16).
This mezzanine checks the CRC of each event, indicates in the trailer if the CRC is wrong and correct the CRC in the case of it is wrong. It sends also to FRL some information like backpressure accumulation time, the frequency used by FED to send data. It will send also a pattern on demand (test link). To do this, the link should leave the DAQ mode and enter in COMMAND mode (controlled by FRL).

At the FRL side, data are input by one or both LVDS connector (LINK 0 & 1). Each link has a buffer of 64Kbytes. Each link is controlled independently, a FPGA controls them and merge events in case of both inputs are used.
Events will be sent to the NIC card by memory segments. Each segment contained a FRL header and a payload. The FRL header informs the NIC on the data (size of data in the segment, last segment, event number, crc error…..).

At the beginning of the system setup, the SLINK should be initialized. To do this, the FRL enter in a COMMAND mode. It can initialize link per link by setting the DC_balance mode ON or OFF, do a DESKEW (if it is necessary), do a test link to check the connection, reset FIFO buffer to have a clear setup before going on.

As soon as the setup is done, the FRL enter in DAQ mode. It is ready to receive data. NIC card sends address segments to FRL……
In the same time that FRL sends data to NIC via the memory segments, data can be spied, a word-count histogram can be built, and status register can be read.

4 FRL Designs

4.1 FRL Design 0

Vendor ID: ECD6; **Device ID**: FF10
R/W: bit can be read and write
R: bit is read only.
W: bit can write '1' or '0', read is '0'

The design 0 is used in normal operation. Data is input by the front connector. The data of the both connectors can be merged or used independently (input 1 or input 2).

Before using the FRL to receive data fragment from FEDs, it should be initialized. In the next paragraphs, the details of each setup will be explained. They will be followed by a description of each functions and a summary table.

4.1.1 SETUP SLINK

In COMMAND mode, setup of the board
In DAQ mode setup to receive data.

4.1.2 PCI Configuration

Offset: 0x0 bit: 15..0 name: Vendor_ID R
This register corresponds to the Vendor ID of the board (function 2 of the card).
Value: ECD6

Offset: 0x0 bit: 31..16 name: Device_ID R
This register correspond to the Device ID of the FRL logic element (function 2 of the card)
Value: FF10

Offset: 0x4 bit: 1 name: Memory space R/W
This bit when set by the BIOS able card to be accessed in memory space.

Offset: 0x4 bit: 2 name: Bus master R/W
This bit when set by the BIOS able the card to do master access on PCI bus

Offset: 0x10 bit: 31..4 name: Base address 0 R/W
This register is write by the BIOS to indicate at which address the card responds to a PCI access

Offset: 0x48 bit: 31..0 name: firmware version R
This register will be increment to the 16 lower bits at each design compilation. The upper 16-bit corresponds to the design number which is 0xF020.

4.1.3 Functions

Offset: 0x0 bit: 31..0 name: setup R/W
This register is used to setup multiple functionalities that are described below.

-Bit 0 : write a 1 to this bit will reset the three Back-pressure counters (see offset 0x180 to 0x194). You don't need to write a zero to this bit.
-Bit 1 : write a '1'to this bit will enable the three back-pressure counters (offset 0x180 to 0x194) to run

Write a zero will disable these counters.

-Bit 15.12: these bits are used as a check when the test link is operating. The value read should change. See below, another counter will replace these bits in the future version (offset 0x174).
-Bit 17: a write to this bit will execute a soft-reset in the FRL logic. All registers will take their default values.
-Bit19: This bit is used to swap or no data send to NIC card. A '0' don't change the data coming from the FED. A '1' will swap all bytes (Header, payload and trailer).
-Bit21: This bit is used to read the result of a test link. When a test link is executed the result is read at the offset 0x5c (see below). The offset 0x5c will return the result of the 32 lower bit when this bit is reset to '0' and the 32 upper bit when this bit is set to '1'.
-Bit 22: In the test link mode this bit return the result of the UCTRL bit. Read a '0' means no error, read a '1' means error on UCTRL SLINK bit.
-Bit 23: This bit is used to read data word by word as a debug mode. The offsets 0x100 to 0x10C are used to read the data when this bit is '1'.
This bit should be '0' for normal functionality.
-Bit 24: Write a '1' to this bit will select the link 0 to be used to receive data from the FED connected to link 0. A '0' will disable the link 0.
-Bit 25: Write a '1' to this bit will select the link 1 to be used to receive data from the FED connected to link 1. A '0' will disable the link 1. Link 1 can be used without using link 0.
-Bit 29: Write a '1' to this bit will deactivate the NIC card. All data coming from the FED is destroyed.
-Bit 30: Write a '1' to this bit if you want to spy all events coming from the FED. The throughput will be reduced because the bandwidth of the Compact PCI is about 70 MB/s.
-Bit 31: Write a '1' to this bit enable the spy mode. The choice of events to spy is done by the bit above or writing event number to spy inside a FIFO (see offset 0x88).

Offset: 0x04 bit: 31..0 name: address block W

This register corresponds to a memory FIFO where NIC should write the NIC memory address of each segment (block) used to transfer event data. This memory segments are free to write data coming from FEDs.

Offset: 0x08 bit: 31..0 name: Histogram R/W

Bit 7..0: these bits set the granularity of the word-count histogram. The table of the granularity is shown in table 1.

Register Value	Granularity
0x01	16 bytes
0x02	32 bytes
0x04	64 bytes
0x08	128 bytes
0x10	256 bytes
0x20	512 bytes

0x40	1024 bytes
0x80	2048 bytes

Table 1: Histogram granularity

Bit 30: This bit should be set to '1' to enable the histogram. When this is '0', the histogram memory is not used for the histogram and the memory content can be used for other purpose.
The memory organization is shown in the Bridge paragraph below.

Bit 31: Write a '1' to this bit reset all the histogram memory content to zero. A read to this bit return a value '0'. You don't need to write '0' to reset it.

Offset: 0x10 bit: 31..0 name: Segment reset R/W

Bit 16: When you write a '1' to this bit the FRL logic will reset the memory FIFO that contains the NIC memory address of each free segment.
Bit 18: When this bit is set to '1', the FRL logic will write a FRL header in each free NIC segment. The bit 29 of the WC word inside the FRL header will be set to '1' to indicate to NIC that it is a segment send back without data and request by this command.

Offset: 0x40 bit: 31..0 name: BX0 R

Read this register return the Bunch Crossing of the current event going through this FRL and coming from the link0.
A write to this register has no effect.

Offset: 0x44 bit: 31..0 name: BX1 R

Read this register return the Bunch Crossing of the current event going through this FRL and coming from the link1.
A write to this register has no effect.

Offset: 0x48 bit: 31..0 name: Trig#_L0 R

Read this register return the Event number of the current event going through the input link 0.
A write to this register has no effect.

Offset: 0x4C bit: 31..0 name: Trig#_L1 R

Read this register return the Event number of the current event going through the input link 1.
A write to this register has no effect.

Offset: 0x50 bit: 9..0 name: Free_S R

Read this register return the number of free segment that FRL still has inside the FIFO.
A write to this register has no effect.

Offset: 0x54 bit: 31..0 name: Rty_PCI R

Read this register return a counter value that accumulates the number of PCI retry done by the NIC card.
A write to this register has no effect. removed

Offset: 0x58 bit: 31..0 name: CMC_ver R

During the test link mode, the compilation version of the SLINK mezzanine card connected to this FRL is send to this register.
A write to this register has no effect.

Offset: 0x5C bit: 31..0 name: TL_Berr R

The result of the test link is return through this register. The data transfer during the test is 64 bit. This register return the 32 lower and 32 upper bit according the bit 21 of the offset 0x00 (see above).

Offset: 0x60 bit: 31..0 name: Debug R

This register is used to return some debug value that can change from one compilation to the other. To have the corresponding bit description, see the summary table below.

Offset: 0x80 bit: 31..0 name: Ld_BS R/W

This register is used to setup the size of the NIC memory segment size. The value is in bytes, but it should be a multiple of 8 bytes (64bit-word). This size includes FRL header and payload.

Offset: 0x84 bit: 4..0 name: Ld_HS R/W

The first 32-bit words of the NIC memory segment are the FRL header. The FRL will write to this header the parameters of the payload (see FRL header description).The size of this header is specified by this register.

Offset: 0x88 bit: 31..0 name: LD_evt_spy W

When the FRL has to spy event it should choose which event to spy. Multiple algorithms can be implemented inside the FRL logic. One of them is to spy event written in a list (a FIFO roll). You can write event number to be spied to this register, they will be written inside a FIFO that will be used as a roll to choose the event number to be spied.

Offset: 0x100 bit: 31..0 name: SlowR0 R

This register is the first of four that are used to read data in slow mode. To use these four registers, the bit 23 of the offset 0x0 should be set to '1'.
This first register read the lower 32 bit of the data coming from FED. The link used is set as in normal functionality.
Read the bit 28 offset 0x60 to know if data is present.

Offset: 0x104 bit: 31..0 name: SlowR1 R

This register corresponds to the 32 upper bits of the data.

Offset: 0x108 bit: 0 name: SlowR2 R

The bit 0 corresponds to the UCTRL control bit of the slink protocol.
Other bits are zeros.

Offset: 0x10C bit: none name: SlowR3 R

The value of this register has no mean. It is used only to increment to the next data word received

Offset: 0x110 bit: 31..0 name: StatusFIFO R

This register gives some values that are useful to debug the setup of the FRL. Data coming from FEDs are buffered inside two 32-bit FIFOs. This register gives some status about these FIFOs. The 32bit word is divided in 4 times 8-bit. The first 8-bit correspond too link 0, the second 8-bit to link 1, the third 8-bit to link2 and the upper 8-bit to link 3 (link 2 and 3 are not used)
Bit 0: if set to '1' the link is selected to read the event. When '0', another link is reading a event.
Bit 1: if set to '1' FIFO1 (corresponding to the lower 32-bit data) is empty. Set to '0' the FIFO is not empty.
Bit 2: if set to '1' FIFO2 (corresponding to the upper 32-bit data) is empty. Set to '0' the FIFO is not empty
Bit 3-4: These bits are used for debugging (masked them)
Bit 5: if set to '0' indicate that a backpressure was occurred. This bit is reset (set to 1) by a soft-reset.
Bit 6: if set to '1' indicate that a SLINK is connected and powered to the link0.
Bit 7: if set to '0' indicate a backpressure. One of the FIFOs is almost full and sends a backpressure to SLINK.
Bit 15..8: identical for link1.
Bit 23..16: 0x00
Bit 31..24: 0x00

Offset: 0x114 bit: 1..0 name: SetSLINKadd R/W

At the initialization of the FRL board, the SLINK should be setup (DC balance, deskew see next).
The SLINK can only setup one link at the time. The link we want to setup is declared with this register.

Value : 0x00 enable link0.
0x01 enable link1
0x10 enable link2
0x11 enable link3

Offset: 0x118 bit: 1..0 name: Deskew R/W

Bit 0: Execute a SLINK LVDS Deskew in the CMC connected to the active LINK activated by the previous offset. When read '0' the deskew command is executed.
Bit 1: set to '1' enable the DESKEW on the FRL side. Reset disables the DEKSEW on the FRL side.

Offset: 0x11C bit: 31..0 name: DAQ mode R/W

The setup the SLINK the FRL is a mode COMMAND and not in DAQ mode. It should be in a mode where FED can't send data. The FRL is then able to send command to the cmc SLINK plugged on the FED. In this mode the DESKEW, DC balance, test link command can be sent to the CMC SLINK.
Bit 0: set to '1' to enter in DAQ mode, reset to '0' to enter in COMMAND mode.
Bit 30: set to '1' execute a partial reset to the buffer FIFO of all links. Read '0' when the reset is executed.
Bit 31: set to '1' execute a global reset to the buffer FIFO of all links. Read '0' when the reset is executed.

Offset: 0x120 bit: 31..0 name: TimerLow R

During the use of the Word-count histogram, a timer of 64-bit is running.
The value of this timer is read but these two registers.
The timer is reset but the histogram reset mode (see above offset 0x30).
A read to this register returns the lower 32-bit.

Offset: 0x124 bit: 31..0 name: TimerHigh R

A read to this register returns the upper 32-bit.

Offset: 0x128 bit: 31..0 name: EventCountL R

The number of event going through the FRL is count by a 64-bit counter.
A soft-reset will reset this counter.
The lower 32-bit value is return by this function.
The upper 32-bit value is return by the next function.

Offset: 0x12C bit: 31..0 name: EventCountH R

The number of event going through the FRL is count by a 64-bit counter.
A soft-reset will reset this counter.
The upper 32-bit value is return by this function.

Offset: 0x130 bit: 1..0 name: TestLink R/W

A test link can be executed (when FRL is set to COMMAND mode) to control the connectivity and to receive the firmware version used in the SLINK mezzanine card connected to the corresponding link. The result of this test and the firmware version are read by offset 0x5C and 0x58.
Write a '1' to bit 0 will start the test link. Write a '0' will stop it.
Write a '1' to bit 1 will reset the register that memorized the SLINK mezzanine firmware version. A read of this bit return 0.

Offset: 0x134 bit: 0 name: DC_balance R/W

Set this bit to '1' enable the DC balance mode of the SLINK, write a '0' disable the DC balance mode of the SLINK (DCbalance mode is explain in the DS90CR484/485 LVDS chip datasheet). To setup this function the FRL should be in COMMAND mode, and the link associate should be activated.

Offset: 0x138 bit: 31..0 name: SegmentCntL R

The number of NIC memory segment used is count in a 64-counter.
This counter is reset with a soft-reset.
The lower 32-bit of the counter is return by the function.

Offset: 0x13C bit: 31..0 name: SegmentCntH R

The number of NIC memory segment used is count in a 64-counter.
This counter is reset with a soft-reset.
The upper 32-bit of the counter is return by the function.

Offset: 0x140 bit: 31..0 name: CRC_SLINK0_L R

The number of CRC error occurred in the slink0 is counter with a 64-bit counter.
This counter is rest with a soft-reset.
The lower 32-bit value is return by this function.

Offset: 0x144 bit: 31..0 name: CRC_SLINK0_H R

The number of CRC error occurred in the slink0 is counter with a 64-bit counter.
This counter is rest with a soft-reset.
The upper 32-bit value is return by this function.

Offset: 0x148 bit: 31..0 name: CRC_SLINK1_L R

The number of CRC error occurred in the slink1 is counter with a 64-bit counter.
This counter is rest with a soft-reset.
The lower 32-bit value is return by this function.

Offset: 0x14C bit: 31..0 name: CRC_SLINK1_H R

The number of CRC error occurred in the slink1 is counter with a 64-bit counter.
This counter is rest with a soft-reset.
The upper 32-bit value is return by this function.

Offset: 0x150 bit: 31..0 name: CRC_FED0_L R

The number of CRC error occurred between FED and SLINK mezzanine in the link0 is counter with a 64-bit counter.
This counter is rest with a soft-reset.
The lower 32-bit value is return by this function.

Offset: 0x154 bit: 31..0 name: CRC_FED0_H R

The number of CRC error occurred between FED and SLINK mezzanine in the link0 is counter with a 64-bit counter.
This counter is rest with a soft-reset.
The upper 32-bit value is return by this function.

Offset: 0x158 bit: 31..0 name: CRC_FED1_L R

The number of CRC error occurred between FED and SLINK mezzanine in the link1 is counter with a 64-bit counter.
This counter is rest with a soft-reset.
The lower 32-bit value is return by this function.

Offset: 0x15C bit: 31..0 name: CRC_FED1_H R

The number of CRC error occurred between FED and SLINK mezzanine in the link1 is counter with a 64-bit counter.
This counter is rest with a soft-reset.
The upper 32-bit value is return by this function.

Offset: 0x160 bit: 31..0 name: BP_link0_L R

Inside the SLINK mezzanine a counter of 44-bit accumulate the backpressure time sent to the FED. This value is send regularly to the FRL.
The lower 32-bit is return but this function.
This counter is reset by the COMMAND mode.
This function corresponds to the FED connected to link0.

Offset: 0x164 bit: 27..0 name: BP_link0_H R

Inside the SLINK mezzanine a counter of 44-bit accumulate the backpressure time sent to the FED. This value is send regularly to the FRL.
Bit 11..0: The upper 12-bit is return but this function.

This counter is reset by the COMMAND mode.
Bit 27..12: return a value that indicates the frequency with which the FED sends data.
This value divided by 100 gives the frequency in MHz.
This function corresponds to the FED connected to link0.

Offset: 0x168 bit: 31..0 name: BP_link1_L R

Inside the SLINK mezzanine a counter of 44-bit accumulate the backpressure time sent to the FED. This value is send regularly to the FRL.
The lower 32-bit is return but this function.
This counter is reset by the COMMAND mode.
This function corresponds to the FED connected to link1.

Offset: 0x16C bit: 27..0 name: BP_link1_H R

Inside the SLINK mezzanine a counter of 44-bit accumulate the backpressure time sent to the FED. This value is send regularly to the FRL.
Bit 11..0: The upper 12-bit is return but this function.
This counter is reset by the COMMAND mode.
Bit 27..12: return a value that indicates the frequency with which the FED sends data.
This value divided by 100 gives the frequency in MHz.
This function corresponds to the FED connected to link1.

Offset: 0x170 bit: 15..0 name: seg_used R

This counter returns the number of NIC segment memory used for the current event.
If both link are used, the event fragment are merged and seen as one.

Offset: 0x174 bit: 31..0 name: Running R

This counter is count each data received either by link0 or link1.
This indicates that something is received by the FRL.
The link activated is indicated by offset 0x110.

Offset: 0x178 bit: 31..0 name: set FED_ID R/W

Bit 11..0: specify the FED_ID for the link0. The event header will be checked with this value, and will report the result in the event trailer bit 0.
Bit 27..16: specify the FED_ID for the link1. The event header will be checked with this value, and will report the result in the event trailer bit 0.

Offset: 0x17C bit: xx name: latch_BP_cnt W

Write to this register will latch the three Backpressure counters to registers

Offset: 0x180 bit: 31..0 name: BP_running_Counter_L R

The function returns the lower part of the 64-bit running counter.
This counter is enabled or disabled by the bit 1 offset 0x0 and reset by the bit 0 offset 0x0.

Offset: 0x184 bit: 31..0 name: BP_running_Counter_H R

The function returns the higher part of the 64-bit running counter.

This counter is enabled or disabled by the bit 1 offset 0x0 and reset by the bit 0 offset 0x0.

Offset: 0x188 bit: 31..0 name: BP_L0_Counter_L R

The function returns the lower part of the 64-bit L0 Backpressure counter. This counter is enabled or disabled by the bit 1 offset 0x0 and reset by the bit 0 offset 0x0.

Offset: 0x18C bit: 31..0 name: BP_L0_Counter_H R

The function returns the higher part of the 64-bit L0 Backpressure counter. This counter is enabled or disabled by the bit 1 offset 0x0 and reset by the bit 0 offset 0x0.

Offset: 0x190 bit: 31..0 name: BP_L1_Counter_L R

The function returns the lower part of the 64-bit L1 Backpressure counter. This counter is enabled or disabled by the bit 1 offset 0x0 and reset by the bit 0 offset 0x0.

Offset: 0x194 bit: 31..0 name: BP_L1_Counter_H R

The function returns the higher part of the 64-bit L1 Backpressure counter. This counter is enabled or disabled by the bit 1 offset 0x0 and reset by the bit 0 offset 0x0.

4.1.4 Summary function table

Function	Base Address	Offset	Bit	R/W	Description
Vendor ID	Conf	0x00	15..0	R	ECD6
Device ID	Conf	0x00	31..16	R	FF10
BA0	Conf	0x10	31..16	R/W	Base address 0
Version	Conf	0x48	31..0	R	The FPGA design version (0xF020xxxx)
BP_cnt_reset	BA0	0x0	0	W	Reset the three Backpressure counters (see offset 0x180 to 0x194)
BP_cnt_ena	BA0	0x0	1	R/W	Enable the three Backpressure counters (see offset 0x180 to 0x194)
Test_run	BA0	0x0	15..12	R	This counter report how many test_link loop were received (should continually looping when test_link is enabled)
Reset	BA0	0x0	17	W	Software reset (by writing a ‘1’ to this bit) Reset all the logic inside the FPGA, excepted the PCI interface
Byte_swap	BA0	0x0	19	R/W	0 = doesn’t swap Event data bytes; 1= Swap Event data bytes
Switch_berr	BA0	0x0	21	R/W	In test_link mode, when ‘0’ we read the 32 bit result (command 0x5C) when ‘1’ , we read the 32 bit high (command 0x5C)
UCTRL_BERR	BA0	0x0	22	R	In test_link mode, this bit is ‘1’ if there is a error on UCTRL bit on SLINK.

Debug mode	BA0	0x0	23	R/W	Slow read acquis. mode . When "1" we can read data coming see offset 0x100 ..0x10C (empty offset 60 bit 28)
Enable link0	BA0	0x0	24	R/W	Write a '1' enable the link 0
Enable link1	BA0	0x0	25	R/W	Write a '1' enable the link 1
Enable link2	BA0	0x0	26	R/W	Write a '1' enable the link 2
Enable link3	BA0	0x0	27	R/W	Write a '1' enable the link 3
Deactivate NIC	BA0	0x0	29	R/W	Deactivate the NIC (write a 1).(FIFO free address segment is always reset when "1".
Spy all events	BA0	0x0	30	R/W	Write a "1" spy all events to the PC
Enable spy	BA0	0x0	31	R/W	Write a "1" enable spy to the PC (events to be spied should be prepared before (with the command 0x88)
Ld_B_add	BA0	0x04	31..0	W	FIFO where the NIC board should write free addresses segment (done by the NIC)
WC_histo	BA0	0x08	31	R/W	Reset values of the histogram WC (by writing a "1")
	BA0	0x08	30	R/W	When "1" the Word count histogram is enabled
	BA0	0x08	7..0	R/W	Set the histo granularity 0x01="16B"; 0x02 = "32 B"; 0x04="64B";….;0x80="2KB"
Free FIFO ptr	BA0	0x10	16	W	Reset all free address segment by writing a '1' to this bit
Flush free FIFO	BA0	0x10	18	R/W	Return free pointers to Myrinet (set the bit 29 o the WC word inside the FRL header)
Current_BX_fed0	BA0	0x40	31..0	R	Current Bunch Crossing (BX) FED0
Current_BX_fed1	BA0	0x44	31..0	R	Current Bunch Crossing (BX) FED1
Crt_trig_l0	BA0	0x48	31..0	R	Current trigger number on link0
Crt_trig_l1	BA0	0x4C	31..0	R	Current trigger number on link1
Nb_blk	BA0	0x50	9..0	R	Number of free segments available for data
Rty_PCI	BA0	0x54	31..0	R	Count how many retry is done by the Myrinet card
Read CMC ver	BA0	0x58	31..0	R	CMC version (available in testlink mode)
	BA0	0x5C	31..0	R	BERR bit High and low word (switched by bit 21 offset 0x00)
Debug	BA0	0x60	1..2	R	Debug SPY mode
	BA0	0x60	22	R	Debug FIFO not empty
	BA0	0x60	23	R	1 = receive event currently
	BA0	0x60	24	R	1 = SPY FULL
	BA0	0x60	25	R	1 = NIC pointers ready
	BA0	0x60	26	R	1 Internal Back pressure (FPGA)
	BA0	0x60	27	R	Receive data for PCI (event bit set)
	BA0	0x60	28	R	1 = not empty (debug mode)
	BA0	0x60	29	R	Transfer FRL header to NIC
	BA0	0x60	30	R	Transfer a event to NIC
	BA0	0x60	31	R	Ready (wait for event)

Ld_BS	BA0	0x80	15..3	R/W	Load the data packet size (bytes) 64bit mult.
Ld_HS	BA0	0x84	4..0	R/W	Load the FRL header size (number of 32-bit words)(usually 0x6)
Ld_evt_spy	BA0	0x88	23..0	W	Load event numbers to be spied (FIFO max. 1024 values))
Slow read	BA0	0x100	31..0	R	Read word 31..0 from link acquis. In Slow read acquis. mode (bit 23 offset 0x00)
	BA0	0x104	31..0	R	Read word 63..32 from link acquis. In Slow read acquis. g mode (bit 23 offset 0x00)
	BA0	0x108	0	R	Bit UCTRL from link acquis. In Slow read acquis. mode (bit 23 offset 0x00)
	BA0	0x10C		R	Reserved word for Slow read acquis.
StatusFIFOs	BA0	0x110	0	R	LINK0 is activated to read events
	BA0	0x110	1	R	LINK0 Fifo0 not empty (1)
	BA0	0x110	2	R	LINK0 Fifo1 not empty (1)
	BA0	0x110	3	R	Used for debuging
	BA0	0x110	4	R	Used for debuging
	BA0	0x110	5	R	Backpressure_memory (reset by soft_reset)
	BA0	0x110	6	R	LINK0 is connected
	BA0	0x110	7	R	Backpressure (real time)
	BA0	0x110	8..12	R	Idem 0..4 for link 1
	BA0	0x110	16..20	R	0x00
	BA0	0x110	24..28	R	0x00
SL_A_SlowCmd	BA0	0x114	1..0	R/W	Set link address to execute (0,1,2,3) Deskew, DCB..on the specified Slink
CMC_DSK	BA0	0x118	0	R/W	Deskew read 0 when finished
FRL_DSK	BA0	0x118	1	R/W	Enable deskew mode (On FRL chips)
DAQ_mode	BA0	0x11C	0	R/W	1 DAQ mode / 0 Command mode (0x114; 0x118)
P_Rst_FF	BA0	0x11C	30	R/W	Partial FIFO reset read 0 when finished
M_Rst_FF	BA0	0x11C	31	R/W	Master FIFO reset read 0 when finished
TimerLow	BA0	0x120	31..0	R	Low 32 bit of timer (uSec)
TimerHigh	BA0	0x124	31..0	R	High 32 bit of timer (uSec)
Evt_counterLow	BA0	0x128	31..0	R	Low 32 bit of event counter
Evt_counterHigh	BA0	0x12c	31..0	R	High 32 bit of event counter
Test_link	BA0	0x130	0	R/W	Test link start 1; end =0 (link set by 0x114)
Rst_Ver#	BA0	0x130	1	W	Write a 1 reset the version number
DC_BAL	BA0	0x134	0	R/W	DC Balance on = 1 off =0 (link set by 0x114)
Seg_nb_cntLow	BA0	0x138	31..0	R	Number of segments (64 bit counter)
Seg_nb_cnt_High	BA0	0x13C	31..0	R	
CRC_L0_Low	BA0	0x140	31..0	R	Number of CRC error on link0 (64 bit counter)
CRC_L0_High	BA0	0x144	31..0	R	
CRC_L1_Low	BA0	0x148	31..0	R	Number of CRC error on link1 (64 bit counter)
CRC_L1_High	BA0	0x14C	31..0	R	
CRC_Fed0_Low	BA0	0x150	31..0	R	Number of CRC error before link0 (64 bit counter)
CRC_Fed0_High	BA0	0x154	31..0	R	
CRC_Fed1_Low	BA0	0x158	31..0	R	Number of CRC error before link1 (64 bit counter)

CRC_Fed1_High	BA0	0x15C	31..0	R	
BP_CNT_L0-L	BA0	0x160	31..0	R	Backpressure counter (link0) low value
BP_CNT_L0-H	BA0	0x164	11..0	R	Backpressure counter (link0) high value
FREQ_MSR_L0	BA0	0x164	27..12	R	FED frequeny (value/ 100 = freqMHz) L0
BP_CNT_L1-L	BA0	0x168	31..0	R	Backpressure counter (link1) low value
BP_CNT_L1-H	BA0	0x16C	11..0	R	Backpressure counter (link1) high value
FREQ_MSR_L1	BA0	0x16C	27..12	R	FED frequeny (value/ 100 = freqMHz) L1
Frag_evt	BA0	0x170	15..0	R	Number of fragment(s) used in current evt yet
CNT_DT_RCV	BA0	0x174	31..0	R	Counter (run when data received on the selecte link
Set_FED_ID0	BA0	0x178	11..0	R /W	Set the FED_ID for link0
Set_FED_ID1	BA0	0x178	27..16	R/W	Set the FED_ID for link1
Latch_BP_cnt	BA0	0x17C		W	Latch the three Backpressure counters in registers. (see offset 0x180 to 0x194)
BP_Running_cntl	BA0	0x180	31..0	R	Running counter lower part
BP_Running_cnth	BA0	0x184	31..0	R	Running counter higher part
BP_L0_cnt_low	BA0	0x188	31..0	R	BP_L0_counter lower part
BP_L0_ cnt_high	BA0	0x18C	31..0	R	BP_L0_counter higher part
BP_L1_ cnt_low	BA0	0x190	31..0	R	BP_L1_counter lower part
BP_L1_ cnt_high	BA0	0x194	31..0	R	BP_L1_counter higher part

4.2 FRL Design I

With the second design we are able to send data to NIC card without FED intervention.
This facility was implemented to give the possibility to use the NIC card (debugging mode, test mode, development mode…) without any connection on the input links.

The event is generated inside the FRL. NIC card has to send two words (offset 0x08) that specified the event.

-the first word .bit 23 ..0 specify the event length (number of 64-bit words; Header and trailer included)
.bit 31..24 FED number

-Second word .bit 23..0 specify the Event number
.bit 31..24 specify the seed for the data generator (pseudo random).

No trigger or other external intervention is needed.
The event is generated with header trailer and a payload that contains pseudo random data.
The 64-bit word is 8 time the same byte. The byte of the first word is '(seed *5) +3' the next will be the result used as seed …etc. It is then possible to regenerate data and the end to check if data are corrupted or no. The CRC included in the Trailer will comfort this check.

With this design, the setup of the link is not needed.

4.2.1 PCI Configuration

Offset: 0x0 bit: 15..0 name: Vendor_ID R

This register corresponds to the Vendor ID of the board (function 2 of the card).
Value: ECD6

Offset: 0x0 bit: 31..16 name: Device_ID R

This register correspond to the Device ID of the FRL logic element (function 2 of the card)
Value: FF10

Offset: 0x4 bit: 1 name: Memory space R/W

This bit when set by the BIOS able card to be accessed in memory space.

Offset: 0x4 bit: 2 name: Bus master R/W

This bit when set by the BIOS able the card to do master access on PCI bus

Offset: 0x10 bit: 31..4 name: Base address 0 R/W

This register is write by the BIOS to indicate at which address the card responds to a PCI access

Offset: 0x48 bit: 31..0 name: firmware version R

This register will be increment to the 16 lower bits at each design compilation. The upper 16-bit corresponds to the design number which is 0xF120.

4.2.2 Functions

Offset: 0x0 bit: 31..0 name: setup R/W

This register is used to setup multiple functionalities that are described below.
-Bit 8: Write this bit to '1', enable PCI interrupt when segment address FIFO is empty.
-Bit 9: Write this bit to '1', enable PCI interrupt when segment address FIFO is half-empty.
-Bit 10: Corresponds to the empty of the segment address FIFO; '0' = empty; '1' = not empty
-Bit 11: Correspond to the half-empty of the segment address FIFO; '0'= half-empty.
-Bit 17 : a write to this bit will execute a soft-reset in the FRL logic. All registers will take their default values.
-Bit19 : This bit is used to swap or no the data send to the optical link card. A '0' don't change the data coming from the FED. A '1' will swap all bytes (Header, payload and trailer).
-Bit 22 : This bit is used to read data word by word as a debug mode. The offset 0x100 to 0x10C are used to read the data when this bit is '1'.
This bit should be '0' for normal functionality.
-Bit 24 : Write a '1' to this bit will select the link 0 to be used to receive data for the FED connected to link 0. A '0' will disable the link 0.
-Bit 25 : Write a '1' to this bit will select the link 1 to be used to receive data for the FED connected to link 1. A '0' will disable the link 1. Link 1 can be used without using link 0.

-Bit 30 : Write a ‘1’ to this bit will able to spy all events coming from the FED. The throughput will be reducing because the bandwidth of the Compact PCI is about 70 MB/s.
-Bit 31 : Write a ‘1’ to this bit enable the spy mode. The choice of events to spy is done by the bit above or writing event number to spy inside a FIFO (see offset 0x88).

Offset: 0x04 bit: 31..0 name: address block W

This register corresponds to a FIFO memory where NIC should write the NIC memory address of each segment (block) used to transfer event data. This memory segments are free to write data coming form FEDs.

Offset: 0x08 bit: 31..0 name: LD_parameters R/W

With this firmware version, events are generated inside the FRL. To do this, the FRL should know the description of the event (size, event#...). With this function, you can write two words to describe each event (see above for details).

Offset: 0x10 bit: 31..0 name: Segment reset R/W

Bit 16 : When you write a ‘1’ to this bit the FRL logic will reset the memory FIFO that contains the address of NIC segments.
Bit 18 : When this bit is set to ‘1’ , the FRL logic will write a FRL header in each free NIC segment. The bit 29 of the WC word inside the FRL header will be set to ‘1’ to indicate to NIC that it is a segment send back without data and request by this command.

Offset: 0x28 bit: 31..0 name: Histogram R/W

Bit 7..0 : these bit set the granularity of the word-count histogram. The table of the granularity is shown in table 1.

Register Value	Granularity
0x01	16 bytes
0x02	32 bytes
0x04	64 bytes
0x08	128 bytes
0x10	256 bytes
0x20	512 bytes
0x40	1024 bytes
0x80	2048 bytes

Bit 30 : This bit should be set to ‘1’ to enable the histogram. When this is ‘0’, the histogram memory is not used for the histogram and the memory content can be used for other purpose.
The memory organization is shown in the Bridge paragraph below.

Bit 31 : Write a ‘1’ to this bit reset all the histogram memory content to zero. A read to this bit return a value ‘0’. You don’t need to write ‘0’ to reset it.

Offset: 0x40 bit: 31..0 name: BX0 R

Read this register return the Bunch Crossing of the current event going through this FRL and coming from the link0.
A write to this register has no effect.

Offset: 0x44 bit: 31..0 name: BX1 R

Read this register return the Bunch Crossing of the current event going through this FRL and coming from the link1.

A write to this register has no effect. (not used because only one link is emulated)

Offset: 0x48 bit: 31..0 name: Trig# R

Read this register return the Event number of the current event going through the FRL.

A write to this register has no effect.

Offset: 0x4C bit: 9..0 name: Free_S R

Read this register return the number of free segment that FRL still has inside the FIFO.

A write to this register has no effect.

Offset: 0x50 bit: 11..0 name: Para_number R

This register is used to return the number of parameter inside de FIFO (these parameters are write with function offset (0x8).

Each event is composed by two words. This means that you are able to send maximum 1024 events parameters (2 words for each event parameters)

The bit 11 indicates when the FIFO is full (set to '1').

Offset: 0x54 bit: 31..0 name: Debug R

This function is use to debug. You can read the last 256 words generated. (UCTRL + upper 31-bit data)

Offset: 0x80 bit: 31..0 name: Ld_BS R/W

This register is used to setup the size of the NIC memory segment size. The value is in bytes, but it should be a multiple of 8 bytes (64bit-word). This size includes FRL header and payload.

Offset: 0x84 bit: 4..0 name: Ld_HS R/W

The first 32-bit words of the NIC memory segment are the FRL header. The FRL will write to this header the parameters of the payload (see FRL header description).The size of this header is specified by this register.

Offset: 0x88 bit: 31..0 name: LD_evt_spy W

When the FRL has to spy event it should choose which event to spy. Multiple algorithms can be implemented inside the FRL logic. One of them is to spy event written in a list (a FIFO roll). You can write event number to be spied to this register, they will be written inside a FIFO that will be used as a roll to choose the event number to be spied.

Offset: 0x100 bit: 31..0 name: SlowR0 R

This register is the first of four that are used to read data in slow mode. To use these four registers, the bit 23 of the offset 0x0 should be set to '1'.

This first register read the lower 32 bit of the data coming from FED. The link used is set as in normal functionality.

Offset: 0x104 bit: 31..0 name: SlowR1 R

This register corresponds to the 32 upper bits of the data.

Offset: 0x108 bit: 0 name: SlowR2 R

This register has only the bit 0 valid. It corresponds to the UCTRL control bit of the slink protocol.

Offset: 0x10C bit: none name: SlowR3 R

The value of this register has no mean. It is used only to increment to the next data word received

Offset: 0x120 bit: 31..0 name: TimerLow R

During the use of the Word-count histogram, a timer of 64-bit is running.
The value of this timer is read but these two regiters.
The timer is reset but the histogram reset mode (see above offset 0x30).
A read to this register returns the lower 32-bit.

Offset: 0x124 bit: 31..0 name: TimerHigh R

A read to this register returns the upper 32-bit.

Offset: 0x128 bit: 31..0 name: EventCountL R

The number of event going through the FRL is count by a 64-bit counter.
A soft-reset will reset this counter.
The lower 32-bit value is return by this function.
The upper 32-bit value is return by the next function.

Offset: 0x12C bit: 31..0 name: EventCountH R

The number of event going through the FRL is count by a 64-bit counter.
A soft-reset will reset this counter.
The upper 32-bit value is return by this function.

4.2.3 Summary function table

Function	Base Address	Offset	Bit	R/W	Description
Vendor ID	Conf	0x00	15..0	R	ECD6
Device ID	Conf	0x00	31..16	R	FF10
BA0	Conf	0x10	31..16	R/W	Base address 0
Version	Conf	0x48	31..0	R	The FPGA design version (0xF120xxxx)
	BA0	0x0	8	R/W	Enable PCI interrupt when segment add fifo is empty
	BA0	0x0	9	R/W	Enable PCI interrupt when segment add fifo is half-empty
	BA0	0x0	10	R	0 = segment add fifo is empty
	BA0	0x0	11	R	0 = segment add fifo is half-empty
Reset	BA0	0x0	17	W	Software reset (by writing a ‘1’ to this bit) Reset all the logic inside the FPGA, excepted the PCI interface
Byte_swap	BA0	0x0	19	R/W	0 = doesn’t swap Event data bytes; 1= Swap

					Event data bytes
Debug mode	BA0	0x0	22	R/W	Slow read acquis. mode . When “1” we can read data coming see offset 0x100 ..0x10C
Enable link0	BA0	0x0	24	R/W	Write a ‘1’ enable the link 0
Enable link1	BA0	0x0	25	R/W	Write a ‘1’ enable the link 1
Enable link2	BA0	0x0	26	R/W	Write a ‘1’ enable the link 2
Enable link3	BA0	0x0	27	R/W	Write a ‘1’ enable the link 3
Spy all events	BA0	0x0	30	R/W	Write a “1” spy all events to the PC
Enable spy	BA0	0x0	31	R/W	Write a “1” enable spy to the PC (events to be spied should be prepared before (with the command 0x88)
Ld_B_add	BA0	0x04	31..0	W	FIFO where the NIC board should write free addresses segment (done by the NIC)
LD_parameters	BA0	0x08	31..0	W	Specify the event to be generated inside the FRL see below for details. Two words should b written by event
Free FIFO ptr	BA0	0x10	16	W	Reset all free address segment by writing a ‘1’ to this bit
Flush free FIFO	BA0	0x10	18	R/W	Return free pointers to Myrinet (set the bit 29 o the WC word inside the FRL header)
WC_histo	BA0	0x28	31	R/W	Reset values of the histogram WC (by writing a “1”)
	BA0	0x28	30	R/W	When “1” the Word count histogram is enabled
	BA0	0x28	7..0	R/W	Set the histo granularity 0x01=”64B”; 0x02 = ”128 B”; 0x04=”256B”;….;0x80=”8KB”
BX_nb_fed0	BA0	0x40	31..0	R	Current BX number FED0
BX_nb_fed1	BA0	0x44	31..0	R	Current BX number FED1
Crt_trig	BA0	0x48	31..0	R	Current trigger number
Nb_blk	BA0	0x4C	8..0	R	Number of free segments available for data
PARA_NB	BA0	0x50	31..0	R	Nomber of events parameters inside FIFO (Number of pending trigger)
Spy Debug fifo	BA0	0x54	31..0	R	Read Spy_debug fifo word (Switch;UCTRL,DT[63..34])
Ld_BS	BA0	0x80	15..3	R/W	Load the data packet size (bytes) 64bit mult.
Ld_HS	BA0	0x84	4..0	R/W	Load the FRL header size (number of 32-bit words)(usually 0x6)
Ld_evt_spy	BA0	0x88	23..0	W	Load event numbers to be spied (FIFO max. 1024 values))
Slow read	BA0	0x100	31..0	R	Read word 31..0 from link acquis. In Slow read acquis. mode (bit 23 offset 0x00)
	BA0	0x104	31..0	R	Read word 63..32 from link acquis. In Slow read acquis. g mode (bit 23 offset 0x00)
	BA0	0x108	0	R	Bit UCTRL from link acquis. In Slow read

					acquis. mode (bit 23 offset 0x00)
	BA0	0x10C		R	Reserved word for Slow read acquis.
StatusFIFOs	BA0	0x110	31..0	R	Read a word in advance from Fifo 1 (1)
TimerLow	BA0	0x120	31..0	R	Low 32 bit of timer (uSec) not yet implemented
TimerHigh	BA0	0x124	31..0	R	High 32 bit of timer (uSec) not yet implemented
Evt_counterLow	BA0	0x128	31..0	R	Low 32 bit of event counter
Evt_counterHigh	BA0	0x12c	31..0	R	High 32 bit of event counter

When we want to generate event inside the FRL (the Input LVDS link is not used). The software has to specify the event to be generated (design I). This is done when we write a data (32 bit) at the offset 0x08:

-the first word .bit 23 ..0 specify the event length (number of 64-bit words; Header and trailer included)

.bit 31..24 FED number

-Second word .bit 23..0 specify the Event number

.bit 31..24 specify the seed for the data generator (pseudo random)

The pseudo random generator creates each data as specified here:
The 64-bit is composed as 8 times identical 8-bit. The first data is the seed multiplied by 5 plus three. The next data is the previous result multiplied by 5 plus 3….etc

4.3 FRL Design II

4.3.1 Description

This firmware version is quite similar to the previous. In this version the description of each event is written inside a memory (see bridge section to see the memory allocated for this).
The request to generate an event is done by an external request (Trigger distributor board in the same backplane), by a PCI access (see below function 0x90) or generate event one after the other without any intervention (PCI access or external request see offset 0x0 bit 15). Each event is described by 2 64-bit words (instead of 2 32-bit words in the previous firmware).
The detail of this description is shown in the table 2.

Function	**Offset**	**Bit**	**Description**
EventLength	0x00	23..0	The length of the event
Source	0x04	11..0	Source number
Seed	0x04	23..16	The seed for payload pseudo random data
BX	0x08	11..0	Bunch Crossing
DeltaT	0x08	31..12	The time before generate the next event 100 ns step
EventID	0x0C	23..0	EventID number (Not used)
ErrorEvID	0x0C	31	Generate a wrong EventID
ErrorCRC	0x0C	30	Generate a wrong CRC

Table 2: Event descriptor

4.3.2 PCI Configuration

Offset: 0x0 bit: 15..0 name: Vendor_ID R

This register corresponds to the Vendor ID of the board (function 2 of the card).
Value: ECD6

Offset: 0x0 bit: 31..16 name: Device_ID R

This register correspond to the Device ID of the FRL logic element (function 2 of the card)
Value: FF10

Offset: 0x4 bit: 1 name: Memory space R/W

This bit when set by the BIOS able card to be accessed in memory space.

Offset: 0x4 bit: 2 name: Bus master R/W

This bit when set by the BIOS able the card to do master access on PCI bus

Offset: 0x10 bit: 31..4 name: Base address 0 R/W

This register is write by the BIOS to indicate at which address the card responds to a PCI access

Offset: 0x48 bit: 31..0 name: firmware version R

This register will be increment to the 16 lower bits at each design compilation. The upper 16-bit corresponds to the design number which is 0xF220.

4.3.3 Functions

Offset: 0x0 bit: 31..0 name: setup R/W

This register is used to setup multiple functionalities that are described below.
-Bit 0 : Corresponds to the empty of the segment address FIFO; '0' = empty; '1' = not empty --Bit 1: Correspond to the half-empty of the segment address FIFO; '0'= half-empty.
-Bit 4: Indicates if the STTS status is READY. It is the signal propagated on the backplane.
-Bit 5: Indicates if the STTS status is BUSY (= !bit 4).
-Bit 8: Write this bit to '1', enable PCI interrupt when segment address FIFO is empty.
-Bit 9: Write this bit to '1', enable PCI interrupt when segment address FIFO is half-empty.
-Bit 10: Write this bit to '1' enable PCI trigger. If this bit is written to '0', a backplane trigger or the bit 15 should bit set to '1' to generate events.
-Bit 12: write a '1' freeze the generation of event (stop where it is no data generated)
Write a '0' release this freeze and continues to generate data.
-Bit 15: Write this bit to '1' if you want events generated without intervention. As soon as the previous is generated the next start, only the internal backpressure will stop momentarily the generator. If you write this bit to '0', a request should be done to generate each event (PCI access or backplane trigger (from trigger distributor board)

-Bit 16: write this bit to '1' will start the generator. Write this bit to '0' will stop it.
-Bit 17: a write to this bit will execute a soft-reset in the FRL logic. All registers will take their default values.
-Bit19: This bit is used to swap or no data send to NIC card. A '0' don't change the data coming from the FED. A '1' will swap all bytes (Header, payload and trailer).
-Bit 23: This bit is used to read data word by word as a debug mode. The offsets 0x100 to 0x10C are used to read the data when this bit is '1'.
This bit should be '0' for normal functionality.
-Bit 24: Write a '1' to this bit will select the link 0 to be used to receive data from the FED connected to link 0. A '0' will disable the link 0.
-Bit 25: Write a '1' to this bit will select the link 1 to be used to receive data from the FED connected to link 1. A '0' will disable the link 1. Link 1 can be used without using link 0.
-Bit 29: Write a '1' to this bit will deactivate the NIC card. All data coming from the FED is destroyed.
-Bit 30: Write a '1' to this bit if you want to spy all events coming from the FED. The throughput will be reduced because the bandwidth of the Compact PCI is about 70 MB/s.
-Bit 31: Write a '1' to this bit enable the spy mode. The choice of events to spy is done by the bit above or writing event number to spy inside a FIFO (see offset 0x88).

Offset: 0x04 bit: 31..0 name: address block W

This register corresponds to a memory FIFO where NIC should write the NIC memory address of each segment (block) used to transfer event data. This memory segments are free to write data coming from FEDs.

Offset: 0x08 bit: 31..0 name: Histogram R/W

Bit 7..0: these bits set the granularity of the word-count histogram. The table of the granularity is shown in table 1.

Register Value	Granularity
0x01	16 bytes
0x02	32 bytes
0x04	64 bytes
0x08	128 bytes
0x10	256 bytes
0x20	512 bytes
0x40	1024 bytes
0x80	2048 bytes

Table 1: Histogram granularity

Bit 30: This bit should be set to '1' to enable the histogram. When this is '0', the histogram memory is not used for the histogram and the memory content can be used for other purpose.
The memory organization is shown in the Bridge paragraph below.

Bit 31: Write a '1' to this bit reset all the histogram memory content to zero. A read to this bit return a value '0'. You don't need to write '0' to reset it.

Offset: 0x10 bit: 31..0 name: Segment reset R/W

Bit 16: When you write a '1' to this bit the FRL logic will reset the memory FIFO that contains the NIC memory address of each free segment.
Bit 18: When this bit is set to '1', the FRL logic will write a FRL header in each free NIC segment. The bit 29 of the WC word inside the FRL header will be set to '1' to indicate to NIC that it is a segment send back without data and request by this command.

Offset: 0x28 bit: 15..0 name: Mask SRAM R/W

The memory used to describe event is huge (!). With this mask you can choose the number of events you want to describe and loop on them. Sixteen values are valid:
0x0001 -> 2 Events
0x0003 -> 4 Events
0x0007 -> 8 Events
0x000F -> 16 Events
0x001F -> 32 Events
..
0xFFFF -> 63536 Events

Offset: 0x40 bit: 31..0 name: BX0 R

Read this register return the Bunch Crossing of the current event going through this FRL and coming from the link0.
A write to this register has no effect.

Offset: 0x44 bit: 31..0 name: BX1 R

Read this register return the Bunch Crossing of the current event going through this FRL and coming from the link1.
A write to this register has no effect. Only the link 0 is emulated

Offset: 0x48 bit: 31..0 name: Trig# R

Read this register return the Event number of the current event going through the FRL.
A write to this register has no effect.

Offset: 0x4C bit: 9..0 name: Free_S R

Read this register return the number of free segment that FRL still has inside the FIFO.
A write to this register has no effect.

Offset: 0x50 bit:8..0 name: Pending trigger R/W

Trigger when external (trigger distributor) can appears faster that the event can be generated.
A counter accumulates triggers and will send a veto to the system if the counter reaches a certain value. The number of pending triggers can be read with this function.

Offset: 0x54 bit: 31..0 name: Debug R

This function is use to debug. You can read the last 256 words generated. (UCTRL + upper 31-bit data)

Offset: 0x80 bit: 31..0 name: Ld_BS R/W

This register is used to setup the size of the NIC memory segment size. The value is in bytes, but it should be a multiple of 8 bytes (64bit-word). This size includes FRL header and payload.

Offset: 0x84 bit: 4..0 name: Ld_HS R/W

The first 32-bit words of the NIC memory segment are the FRL header. The FRL will write to this header the parameters of the payload (see FRL header description).The size of this header is specified by this register.

Offset: 0x88 bit: 31..0 name: LD_evt_spy W

When the FRL has to spy event it should choose which event to spy. Multiple algorithms can be implemented inside the FRL logic. One of them is to spy event written in a list (a FIFO roll). You can write event number to be spied to this register, they will be written inside a FIFO that will be used as a roll to choose the event number to be spied.

Offset: 0x90 bit: name: PCI trigger W

A write to this function will generate a trigger. An event will be generated as soon as possible.
The data has no mean. Only write is valid. A read return a zero and has no action.
To be valid the bit 10 offset 0x0 should be set to '1'.

Offset: 0x94 bit: name: CRC_gen W

A write to this function will generate a CRC error for the next event. The data has no mean. Only write is valid. A read return a zero and has no action.

Offset: 0x98 bit:31..0 name: LD_evt R/W

The event number used to generate the event can be initialized with this function. This register is incremented by the trigger signal. To use this register as trigger number, the bit 11 offset 0x0 should be set to '1'.

Offset: 0x9C bit:3..0 name: Outsync_gen W

A write to this function generates an out-of-sync.
Actually four outsync are distinguished. The bit selects which one you want to generate.
Bit0: One event, with a wrong event#, is inserted between two events.
Ex: 1. 2. 3. 100. 4. 5. 6. ….
Bit1: One event, with a wrong event#, replaced one event.
Ex: 1. 2. 3. 100. 5. 6. ….
Bit2: One event is missing.
Ex: 1. 2. 3. 5. 6. …..
Bit3: the serial event# are changed
Ex: 1. 2. 3. 100. 101. 102. 103. 104. ….

In the example, the event number inserted is 100. In the reality, the event number is the complementary of the actual one. Later we can imagine that the function specify the event number used.

Offset: 0xA0 bit:0 name: Resync W

Write a '1' to the bit 0 of this function resync the system.

The current event is finished then:
The pending trigger counter is reset and the Event number counter is set to '1'.

Offset: 0xA4 bit:8..0 name: Thre_ready R/W

To control the trigger system, the signal ready/busy is controlled with a hysteresis. The threshold for ready is load via this function.

Offset: 0xA8 bit:8..0 name: Thre_busy R/W

To control the trigger system, the signal ready/busy is controlled with a hysteresis. The threshold for busy is load via this function.

Offset: 0xAC bit:1..0 name: Thre_busy R/W

These two bit control the generation of STTS signals (BUSY/READY). To control the STTS BUSY READY by PCI bit0 should be set to '1'. If the bit is set to '0', the normal function is activated (threshold and pending triggers).
Bit 1 set to '1'generate a BUSY on the backplane (propagated to the Trigger distributor board and to FMM board).
Bit 1 set to '0' generate a READY level.

Offset: 0x100 bit: 31..0 name: SlowR0 R

This register is the first of four that are used to read data in slow mode. To use these four registers, the bit 23 of the offset 0x0 should be set to '1'.
This first register read the lower 32 bit of the data coming from FED. The link used is set as in normal functionality.

Offset: 0x104 bit: 31..0 name: SlowR1 R

This register corresponds to the 32 upper bits of the data.

Offset: 0x108 bit: 0 name: SlowR2 R

The bit 0 corresponds to the UCTRL control bit of the slink protocol.
Other bits are zeros.

Offset: 0x10C bit: none name: SlowR3 R

The value of this register has no mean. It is used only to increment to the next data word received

Offset: 0x110 bit: none name: SLINK_Status R

Bit4: data are present in the internal FPGA. This bit can be used to know if data are present in debug mode (func0x100-0x10C).
Bit 5: Indicate that a backpressure was occurred . This bit is reset by a soft-reset.
Bit7: Indicate that a backpressure is currently active.

Offset: 0x120 bit: 31..0 name: TimerLow R

During the use of the Word-count histogram, a timer of 64-bit is running.
The value of this timer is read but these two registers.
The timer is reset but the histogram reset mode (see above offset 0x30).
A read to this register returns the lower 32-bit.

Offset: 0x124 bit: 31..0 name: TimerHigh R

A read to this register returns the upper 32-bit.

Offset: 0x128 bit: 31..0 name: EventCountL R

The number of event going through the FRL is count by a 64-bit counter.
A soft-reset will reset this counter.
The lower 32-bit value is return by this function.
The upper 32-bit value is return by the next function.

Offset: 0x12C bit: 31..0 name: EventCountH R

The number of event going through the FRL is count by a 64-bit counter.
A soft-reset will reset this counter.
The upper 32-bit value is return by this function.

Offset: 0x138 bit: 31..0 name: SegmentCntL R

The number of NIC memory segment used is count in a 64-counter.
This counter is reset with a soft-reset.
The lower 32-bit of the counter is return by the function.

Offset: 0x13C bit: 31..0 name: SegmentCntH R

The number of NIC memory segment used is count in a 64-counter.
This counter is reset with a soft-reset.
The upper 32-bit of the counter is return by the function.

4.3.4 Summary function table

Function	Base Address	Offset	Bit	R/W	Description
Vendor ID	Conf	0x00	15..0	R	ECD6
Device ID	Conf	0x00	31..16	R	FF10
BA0	Conf	0x10	31..16	R/W	Base address 0
Version	Conf	0x48	31..0	R	The FPGA design version (0xF220xxxx)
	BA0	0x0	0	R	1 Myrinet segment address present; 0 empty
	BA0	0x0	1	R	1 Myrinet segment address fifo half full
	BA0	0x0	4	R	READY STTS signal
	BA0	0x0	5	R	BUSY STTS signal
	BA0	0x0	8	R/W	Enable PCI interrupt when Myr seg address fifo is half_empty
	BA0	0x0	9	R/W	Enable PCI interrupt when Myr seg address fifo is empty
	BA0	0x0	10	R/W	Enable PCI trigger
	BA0	0x0	12	R/W	1 freeze the data generator
	BA0	0x0	15	R/W	1 generate events without triggers
	BA0	0x0	16	R/W	Start event generator
Reset	BA0	0x0	17	W	Software reset (by writing a ‘1’ to this bit) Reset all the logic inside the FPGA, excepted the PCI interface
Byte_swap	BA0	0x0	19	R/W	0 = doesn’t swap Event data bytes; 1= Swap

					Event data bytes
Debug mode	BA0	0x0	23	R/W	Slow read acquis. mode . When “1” we can read data coming see offset 0x100 ..0x10C
Enable link0	BA0	0x0	24	R/W	Write a ‘1’ enable the link 0
Enable link1	BA0	0x0	25	R/W	Write a ‘1’ enable the link 1
Enable link2	BA0	0x0	26	R/W	Write a ‘1’ enable the link 2
Enable link3	BA0	0x0	27	R/W	Write a ‘1’ enable the link 3
Deactivate NIC	BA0	0x0	29	R/W	Deactivate the NIC (write a 1).(FIFO free address segment is always reset when “1”.
Spy all events	BA0	0x0	30	R/W	Write a “1” spy all events to the PC
Enable spy	BA0	0x0	31	R/W	Write a “1” enable spy to the PC (events to be spied should be prepared before (with the command 0x88)
Ld_B_add	BA0	0x04	31..0	W	FIFO where the NIC board should write free addresses segment (done by the NIC)
WC_histo	BA0	0x08	31	R/W	Reset values of the histogram WC (by writing a “1”)
	BA0	0x08	30	R/W	When “1” the Word count histogram is enabled
	BA0	0x08	7..0	R/W	Set the histo granularity 0x01=”64B”; 0x02 = ”128 B”; 0x04=”256B”;….;0x80=”8KB”
				R/W	
Free FIFO ptr	BA0	0x10	16	W	Reset all free address segment by writing a ‘1’ to this bit
Flush free FIFO	BA0	0x10	18	R/W	Return free pointers to Myrinet (set the bit 29 o the WC word inside the FRL header)
LD_mask	BA0	0x28	15..0	R/W	Load the memory space mask used for the even parameters (0x1= 2 evt; 0x3= 4 evt; 0x7=8evt; ..)
BX_nb_fed0	BA0	0x40	31..0	R	Current BX number FED0
BX_nb_fed1	BA0	0x44	31..0	R	Current BX number FED1
Crt_trig	BA0	0x48	31..0	R	Current trigger number
Nb_blk	BA0	0x4C	8..0	R	Number of free segments available for data
Pend_trig	BA0	0x50	8..0	R	Number of pending trigger
Spy Debug fifo	BA0	0x54	31..0	R	Read Spy_debug fifo word (Switch;UCTRL,DT[63..34])
Ld_BS	BA0	0x80	15..3	R/W	Load the data packet size (bytes) 64bit mult.
Ld_HS	BA0	0x84	4..0	R/W	Load the FRL header size (number of 32-bit words)(usually 0x6)
Ld_evt_spy	BA0	0x88	23..0	W	Load event numbers to be spied (FIFO max. 1024 values))
PCI_trig	BA0	0x90		W	Generate a PCI trigger
CRC_err	BA0	0x94		W	Generate a CRC error in the next event
Ld_evt	BA0	0x98	31..0	R/W	Load the first event number

OutSync-gen	BA0	0x9C	3..0	W	Generate differents OutOfSync
Resync	BA0	0xA0	0	W	Resync request
Th_ready	BA0	0xA4	8..0	R/W	Thresold for ready signal
Th_Busy	BA0	0xA8	8..0	R/W	Thresold for busy signal
Gen_STTS	BA0	0xAC	1..0	R/W	Generate STTS signal
Slow read	BA0	0x100	31..0	R	Read word 31..0 from link acquis. In Slow read acquis. mode (bit 23 offset 0x00)
	BA0	0x104	31..0	R	Read word 63..32 from link acquis. In Slow read acquis. g mode (bit 23 offset 0x00)
	BA0	0x108	0	R	Bit UCTRL from link acquis. In Slow read acquis. mode (bit 23 offset 0x00)
	BA0	0x10C		R	Reserved word for Slow read acquis.
SLINK_Status	BA0	0x110	4..7	R	Slink status
TimerLow	BA0	0x120	31..0	R	Low 32 bit of timer (uSec) not yet implemented
TimerHigh	BA0	0x124	31..0	R	High 32 bit of timer (uSec) not yet implemented
Evt_counterLow	BA0	0x128	31..0	R	Low 32 bit of event counter
Evt_counterHigh	BA0	0x12c	31..0	R	High 32 bit of event counter
Seg_numberLow	BA0	0x138	31..0	R	Low 32 bit of segment numbers
Seg_numberHigh	BA0	0x13C	31..0	R	High 32 bit of segment numbers

5 Bridge Design

5.2 Description

The bridge FPGA has multiple applications:
-It is the element that interface the CompactPCI bus (32-bit 33MHz) with the internal PCI bus (64-bit 66MHz).
-It controls the SPY function, the memory shared between him and the main FRL FPGA contain spied event that is read by the bridge and sent to the PC memory.
-It controls the JTAG bus to reload the Flash memory and EEPROM that contain FPGA firmwares.
-It controls the access to the memory. Reads histogram and fills the memory with event descriptors when we use the FRL firmware number III.

The three FRL PCI functions are control by the bridge (Bridge, FRL, NIC card). Each access coming from the CompactPCI bus is kept by the bridge or transfer to the internal bus.

The JTAG function is done via memory access. The enable of the JTAG bus is done with the bit 0 of the configuration offset 0x40. Four registers control the JTAG bus:
JTAG_DTE : specifies bits valid (1 to 32 bit)
JTAG_TDI : correspond to the TDI bit to be shifted. Bits valid are indicated by JTAG_DTE)
JTAG_TMS: correspond to the TMS bit to be shifted. (Bits valid are indicated by JTAG_DTE)
JTAG_TDO: is the TDO bit shifted during the access.
The JTAG shift is started by the access JTAG_TDI.

5.3 Spy function

The spy function is a logic that sends events (write access) to the PC memory controlling the CompactPCI backplane.
This PC has a part of memory divided in blocks. The address blocks are sent to a FIFO inside the bridge. As soon as data are available inside the memory (shared between bridge and the main FRL Bridge), the bridge send data using the memory blocks given by the PC. At the end of the event, the bridge send the event size to a FIFO implemented by the PC (pointer of this FIFO is controlled by the PC itself).

5.4 PCI configuration

Offset: 0x0 bit: 15..0 name: Vendor_ID R

This register corresponds to the Vendor ID of the board (function 2 of the card).
Value: ECD6

Offset: 0x0 bit: 31..16 name: Device_ID R

This register correspond to the Device ID of the FRL logic element (function 2 of the card)
Value: FF01

Offset: 0x4 bit: 1 name: Memory space R/W

This bit when set by the BIOS able card to be accessed in memory space.

Offset: 0x4 bit: 2 name: Bus master R/W

This bit when set by the BIOS able the card to do master access on PCI bus

Offset: 0x10 bit: 31..0 name: Base address 0 R/W

This register is write by the BIOS to indicate at which address the card responds to a PCI access.

Offset: 0x40 bit: 18..0 name: JTAG_ctrl R/W

This register controls the JTAG :
-bit 0: Sets this bit to '1' to control the JTAG bus via software. This bit should bit reset to '0' if you want to plug the JTAG controller in the connector on the back of the board. The PCI configuration should be read before the reload to avoid rebooting the PC. A soft-reset should be executed inside the bridge and the PCI configuration rewrite.
-bit 1: writes this bit to '1' will reload the bridge FPAG with the firmware inside the EEPROM. The PCI configuration should be read before the reload to avoid rebooting the PC. A soft-reset should be executed inside the bridge and the PCI configuration rewrite.

-bit 2: writes this bit to '1' will reload the main FRL FPGA with the firmware inside the flash memory. The design to be uploading is specified by the bit 18..16 (see below)
-bit18..16: these 3 bits are used to specify the design we want to upload inside the main FRL FPGA. Four different designs are available.

Offset: 0x48 bit: 31..4 name: firmware version R

This register will be increment to the 16 lower bits at each design compilation. The upper 16-bit corresponds to the design number.

Offset: 0x50 bit: 4..0 name: Geo_add R

This register returns the geographical address of the board. It is useful to know the slot position of the board inside the CompactPCI backplane.

Offset: 0x5C bit: 31..0 name: SNa R

This register returns the lower 32-bit of the board serial number.

Offset: 0x60 bit: 31..0 name: SNb R

This register returns the bit 63 to 32 of the board serial number.

Offset: 0x64 bit: 11..0 name: SNc R

This register returns the upper 12-bit of the board serial number.

5.5 Functions

Offset: 0x0 bit: 31..0 name: setup R/W

This register is used to setup multiple functionalities that are described below.
-Bit 0 : Corresponds to the empty of the free address blocks (SPY function). FIFO; '0' = empty; '1' = not empty
-Bit 1: Correspond to the half-empty of the free address blocks (SPY function). FIFO; '0'= half-empty.
-Bit 8: Write this bit to '1', enable PCI interrupt when address blocks FIFO is empty (SPY function).
-Bit 9: Write this bit to '1', enable PCI interrupt when address blocks FIFO is half-empty (SPY function).
-Bit 10: Write this bit to '1' enables the SPY mode. As soon as data will be valid and address blocks available, the Bridge will send data spied to the PC memory.
-Bit 17: a write to this bit will execute a soft-reset in the FRL logic. All registers will take their default values.

Offset: 0x04 bit: 31..0 name: address block W

This register corresponds to a memory FIFO where PC should write the address of each blocks of memory used to transfer spied data. This memory blocks are free to write data coming from the spy mode. The FIFO is able to contain up to 64 address block.

Offset: 0x80 bit: 31..0 name: Ld_BS R/W

This register is used to setup the size of the memory block size (SPY mode). The value is in bytes, but it should be a multiple of 8 bytes (64bit-word).

Offset: 0x84 bit: 31..0 name: Ld_add_FF R/W

When an event spied is sent to the PC memory (via memory blocks), the bridge send the event size to a PC FIFO. The address of the FIFO is set by this function.

Offset: 0x88 bit: 31..0 name: add_FF_pw W

To inform that the bridge has written a value inside the PC FIFO, it should update the write pointer. The address of the write pointer is set by this function.

Offset: 0x8090 bit:31..0 name: JTAG_TDE R/W

Write to this register the bit available to be shifted in a JTAG access. A bit is care for the shift when it is set to '1'. The bit available should start from the lower bit (bit 0) without hole. As soon as a bit is '0' the bits upper will be ignored. This register should not be reloaded at each time if it doesn't change.

Offset: 0x8094 bit: 31..0 name: JTAG_TDI R/W

This register loads TDI bits to be shifted in a JTAG access. A write access to this register will start a JTAG shift access. Other JTAG register should load before.

Offset: 0x8098 bit: 31..0 name: JTAG_TMS R/W

This register loads the TMS bits to be shifted during a JTAG access. This register should not be reloaded at each time if it doesn't change.

Offset: 0x809C bit: 0 name: JTAG_TDO R

This register return the TDO bit shifted during a JTAG access. When a JTAG access is initiated by JTAG_TDI function (offset 0x8094). The access to JTAG_TDO will generate a PCI retry if the software try to read it and the JTAG access is not finished.

Offset: 0x200000 to 0x3FFFFF bit: 31..0 name: Memory R/W

This offsets access the memory (shared by both FPGA) to read and write histogram, event descriptors…(see 5.6 for the memory map)

5.6 Summary functions table

Function	Base Address	Offset	Bit	R/W	Description
Vendor ID	Conf	0x00	15..0	R	ECD6
Device ID	Conf	0x00	31..16	R	FF01
BA0	Conf	0x10	31..16	R/W	Base address 0
BA1	Conf	0x10	31..22	R/W	Base address 1
JTAG_ena	Conf	0x40	0	R/W	Write a '1' enable drive the JTAG bus with the FPGA
Relaod_B	Conf	0x40	1	R/W	Write a '1' reload the Bridge FPGA with the EEPROM content
Relaod F	Conf	0x40	2	R/W	Write a '1' reload the FRL FPGA with the Memory Flash content (specified by the add_flash (command see below)
Add_flash	Conf	0x40	18..16	R/W	Specify the design to be reload in the FRL FPGA (000= design 0, 001= design 1, 010= design 2….)
Version	Conf	0x48	31..0	R	The FPGA design version
GA	Conf	0x50	4..0	R	Geographic address of the FRL, *(0= System board, 1= second slot starting from right side…. To be confirm with the*

					last crate version)
Serial_N0	Conf	0x5C	31..0	R	Serial number bit 31..0
Serial_N1	Conf	0X60	31..0	R	Serial number bit 63..32
Serial_N2	Conf	0x64	11..0	R	Serial number bit 75..64
Ptr_ff_empty	BA0	0x00	0	R	1 = FIFO pointers is empty
Ptr_ff_H_empty	BA0	0x00	1	R	1 = FIFO pointers is half empty
Ena_INTA_E	BA0	0x00	8	R/W	Enable interruption when FIFO pointer is empty
Ena_INTA_HE	BA0	0x00	9	R/W	Enable interruption when FIFO pointer is half empty
Spy_ena	BA0	0x00	10	W	Set the spy mode
Reset	BA0	0x00	17	W	Software reset
LD_Add_B	BA0	0x4	31..0	W	Load the data block address (max. 64 blocks)
Ld_BS	BA0	0x80	15..2	R/W	Load the block size (bytes), 32bit mult.
Ld_add_FF	BA0	0x84	31-12	R/W	Load the FIFO base address for Event WC
Ld_FF_ptr_A	BA0	0x88	31..0	R/W	Address to update the FIFO write pointer
ZBT_mem	BA0	0x200000-0x3FFFFF	31..0	R/W	The ZBT memory (for histograms)
JTAG_DTE		0x8090	31..0	R/W	Specify Which bit are valid (starting by bit 0)
JTAG_TDI		0x8094	31..0	R/W	Write up to 32 TDI bit (valid bits are masked by JTAG_DTE). Bit 0 is shifted first. A write to this register start the JTAG register shift.
JTAG_TMS		0x8098	31..0	R/W	Write up to 32 TMS bit (valid bits are masked by JTAG_DTE)
JTAG_TDO		0x809C	31..0	R	Read TDO bit up to 32 bit (number of bit masked by JTAG_DTE

5.7 Memory Map

The memory shared between both FPGA is divided in 3 elements:
-The memory to spy event (not seen by the PC)
-The histogram memory
-The event descriptor (for FPGA design II)

Histogram:
There are two tables, one for each link (link0 & link1)

LINK0
The 256 histogram points (32-bit) for link0 start at offset 0x200000 to 0x2003FC .
At the offset 0x200400, there is the overflow (All events bigger that the last point in table above).
At the offset 0x200404, there is the FED# corresponding to the link0.
At the offset 0x200408, there is the lower part of word counter (accumulation word-count of each event, number of 64-bit word).
At the offset 0x20040C, there is the higher part of the word counter.
From offset 0x204000 to 0x207FFC the is the BX histogram (4096 points x 32-bit)

LINK1
The 256 histogram points (32-bit) for link1 start at offset 0x280000 to 0x2803FC.
At the offset 0x280400 , there is the overflow (All events bigger last point in table above)
At the offset 0x280404, there is the FED# corresponding to the link1
At the offset 0x280408, there is the lower part of word counter (accumulation word-count of each event, number of 64-bit word).
At the offset 0x28040C, there is the higher part of the word counter.
From offset 0x284000 to 0x287FFC the is the BX histogram (4096 points x 32-bit)

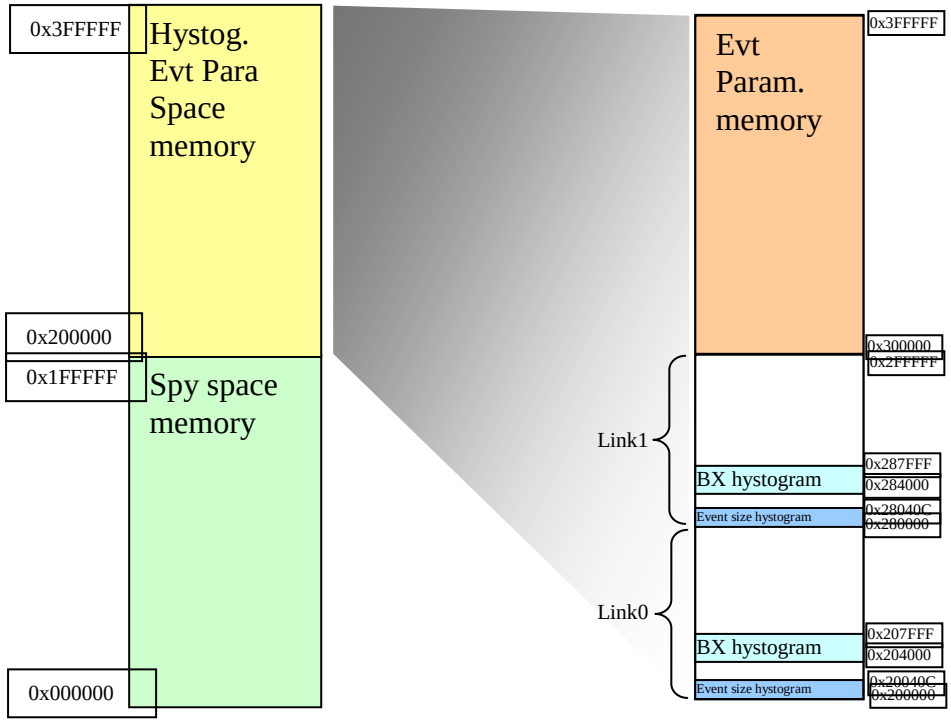

Figure 1: ZBT Memory

The memory space from 0x300000 to 0x3FFFFF is for the event descriptor memory (Design II).
Each event is described by two 64-bit words:

Function	**Offset**	**Bit**	**Description**
EventLength	0x00	23..0	The length of the event (in bytes)
Source	0x04	11..0	Source number

Seed	0x04	23..16	The seed for payload pseudo random data
BX	0x08	11..0	Bunch Crossing
DeltaT	0x08	31..12	The time before generate the next event 100 ns step
EventID	0x0C	23..0	EventID number (not used)
ErrorEvID	0x0C	31	Generate a wrong EventID
ErrorCRC	0x0C	30	Generate a wrong CRC

The number of event descriptors can be 2, 4, 8, 16,… and are specify by the mask offset 0x08 in the FRL space address (design II).

ANNEXE A

This section corresponds to the description of the GIII used to test the production of the FRL and SLINK CMC cards.
Details can be finding in the manual written by Dirk Samyn

GenerciIII (FED-emu & Myrinet-emu)

Vendor ID: ECD6 ; Device ID: FE11
This generator is used to work with a GIII plugged on the FRL.
For the FED-EMU see here

Function	Base Address	Offset	Bit	R/W	Description
Reset	BA0	0x00	17	W	Software reset
Evt_preload	BA0	0x00	7	R/W	Memory filled with real event (no generator)
Step_evt	BA0	0x00	8	R/W	Sent one evt in step mode
Start	BA0	0x00	10	R/W	Start to generate events
Step_ena	BA0	0x00	11	W	Send one event (if bit 8 set to 1)
Set_dt_gen	BA0	0x00	12	R/W	(1) data is gen. (0) pattern is used
Stop_on_err	BA0	0x00	13	R/W	Stop on error if 1
Disable_timer	BA0	0x00	14	R/W	Disable timer between Evt if 1
Ld_A_PFF	BA0	0x04	31..0	R/W	Correspond to the BA0 (FRL +off 0x04)
Ld_mask	BA0	0x08	21..0	R/W	Load the mask for number of events in event descriptor SDRAM (0,1,3,7,F,1F….)
Ld_mask_pat	BA0	0x10	7..0	R/W	Load the mask for pattern payload to be used
Ld_BS	BA0	0x80	15..3	R/W	Load the data packet size (bytes) 64bit mult.
Err_dt	BA0	0x14	31..0	R	Number of error(s) in data
Err_HD	BA0	0x18	31..0	R	Number of error(s) in header
Err_bit_L	BA0	0x1c	31..0	R	Indicate the wrong bit (data 31..0)
Err_bit_H	BA0	0x20	31..0	R	Indicate the wrong bit (data 63..32)
Event_cnt	BA0	0x24	31..0	R	Number of events sent
dt_r_low	BA0	0x28	31..0	R	FIFO 32 w of dt31..0 received
dt_g_low	BA0	0x2c	31..0	R	FIFO 32 w of dt31..0 generated
dt_r_high	BA0	0x30	31..0	R	FIFO 32 w of dt63..32 received
dt_g_high	BA0	0x34	31..0	R	FIFO 32 w of dt63..32 generated
Err_code	BA0	0x50	31..0	R	Error code to be defined
Err_code_bis	BA0	0x54	31..0	R	
	BA0	0x94	0	W	Generate a CRC error on next event
	BA0	0x94	1	W	Generate an event without Trailer
STTS_ENA	BA0	0xA0	4	R/W	0 user the threshold and eFED logic to drive STTS signals; 1 use the register to set READY, OVERFLO….
STTS_OV	BA0	0xA0	0	R/W	Setup overflow signal (bit 4 = 1)
STTS_OS	BA0	0xA0	1	R/W	Setup outsync signal (bit 4 = 1)
STTS_BS	BA0	0xA0	2	R/W	Setup busy signal (bit 4 = 1)
STTS_RD	BA0	0xA0	3	R/W	Setup ready signal (bit 4 = 1)
STTS_RD_Th	BA0	0xA4	7..0	R/W	Set threshold for READY
STTS_BS_Th	BA0	0xA8	7..0	R/W	Set threshold for BUSY

	BA0	0xAc	0	R/W	
Ld_pat	BA0	0x8000-0x83FF	31..0	R/W	Load the 64-bit patterns paylaod (128 patterns)
Evt_Par	BA1	0x000000-0x1FFFFFF	31..0	R/W	SDRAM for the event descriptors (32 MB)
FRL_check	BA2	0x000000-0xFFFFFF	31..0	R/W	Address space where FRL writes back data

FRL Header
Five 32-bit words transferred as header at the beginning of a Myrinet memory segment (Block)

First word:	FED number	[11..0]
Second word:	trigger number	[23..0]
Third word:	Packet number	[15..0]
Fourth word:	reserved	
Fifth word:	Word count	[26..0] (byte unit)
	CRC error in FED	28
	Flush bit	29
	CRC error on SLINK	30
	EOF event	31